Traineeships in Advanced Computing for High Energy Physics (TAC-HEP)

GPU & FPGA module training: Part-2

Week-6: LHC, CMS Level-1 Trigger, Project

Lecture-11: April 25th 2023

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So Far…

- **FPGA and its architecture**
  - Registor/Flip-Flops, LUTs/Logic Cells, DSP, BRAMs
  - Clock Frequency, Latency
  - Extracting control logic & Implementing I/O ports
- **Parallelism in FPGA**
  - Scheduling, Pipelining, DataFlow
- **Vivado HLS**
  - Introduction, Setup, Hands-on for GUI/CLI, Introduction to Pragmas
  - Different Pragmas and their effects on performance
  - Practices to follow while writing HLS code – do's & don'ts

Today:

- LHC, CMS Experiment
- Level-1 Trigger
- Project

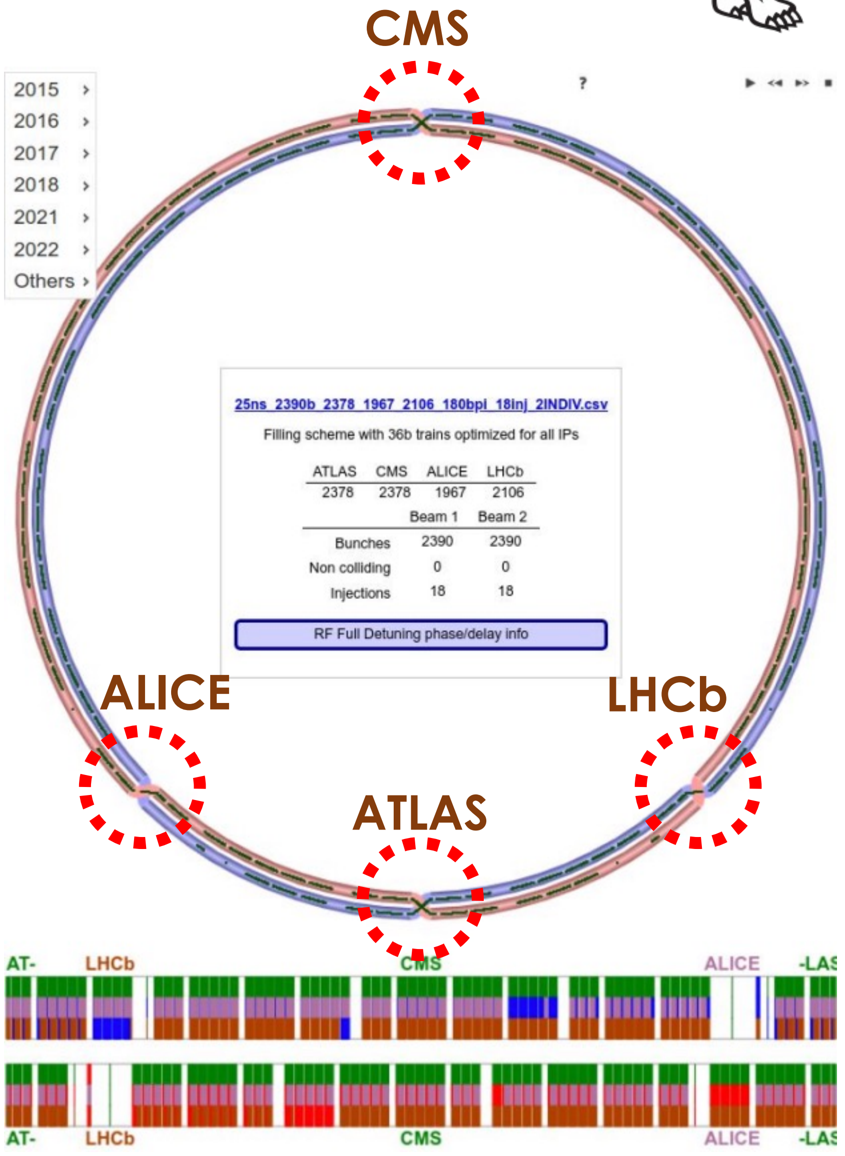
LHC, CMS Experiment

Large Hadron Collider

The LHC accelerates bunches of millions of protons (or ions) from 450 GeV injection energy from SPS to 6.8 TeV and collides them at **13.6 TeV** centre-of-mass energy

LHC circumference is 27 km and the minimal distance between bunches is 25 ns * c

- Revolution frequency of LHC is 11.24 kHz
- Bunch crossing rate (ZeroBias rate) depends on number of bunches in the machine
- E.g. For 2380 colliding bunches (2023)
  - ZeroBias rate = 26.8 MHz



25ns_2390b_2378_1967_2106_180bpi_18inj_2INDIV.csv

Filling scheme with 36b trains optimized for all IPs

ATLAS	CMS	ALICE	LHCb
2378	2378	1967	2106

	Beam 1	Beam 2
Bunches	2390	2390
Non colliding	0	0
Injections	18	18

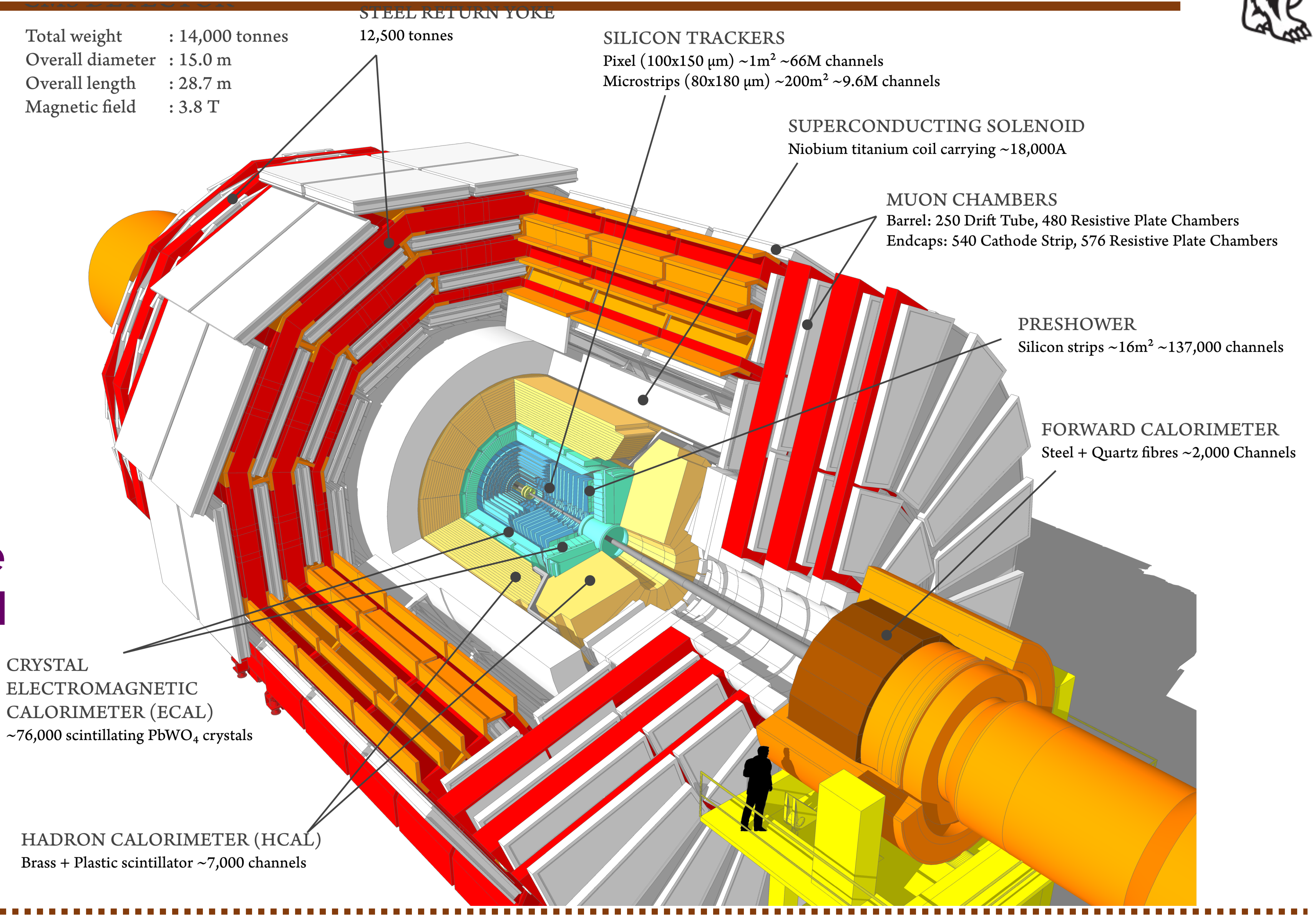
RF Full Detuning phase/delay info

CMS Detector

The LHC collides bunches of protons at **40 MHz***

We can’t readout all collisions (Zero suppressed data would be ~30TB/s)

Primary requirement of the CMS detector is to store all interesting events (data)



Total weight : 14,000 tonnes
Overall diameter : 15.0 m
Overall length : 28.7 m
Magnetic field : 3.8 T

STEEL RETURN YOKE
12,500 tonnes

SILICON TRACKERS
Pixel (100x150 μm) ~1m² ~66M channels
Microstrips (80x180 μm) ~200m² ~9.6M channels

SUPERCONDUCTING SOLENOID
Niobium titanium coil carrying ~18,000A

MUON CHAMBERS
Barrel: 250 Drift Tube, 480 Resistive Plate Chambers
Endcaps: 540 Cathode Strip, 576 Resistive Plate Chambers

PRESHOWER
Silicon strips ~16m² ~137,000 channels

FORWARD CALORIMETER
Steel + Quartz fibres ~2,000 Channels

CRYSTAL ELECTROMAGNETIC CALORIMETER (ECAL)
~76,000 scintillating $PbWO_4$ crystals

HADRON CALORIMETER (HCAL)
Brass + Plastic scintillator ~7,000 channels

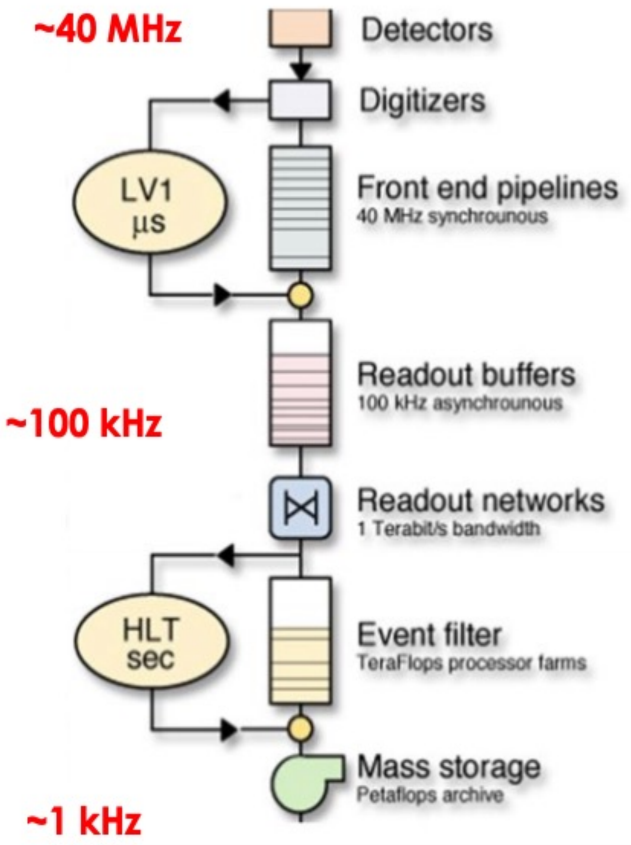
CMS Trigger

CMS cannot readout the full raw detector data (RAW) in all bunch crossings (~40 MHz)

CMS Trigger: Reduces the event rate from the LHC collision rate to what can be stored and analysed offline while keeping the physics reach of the experiment

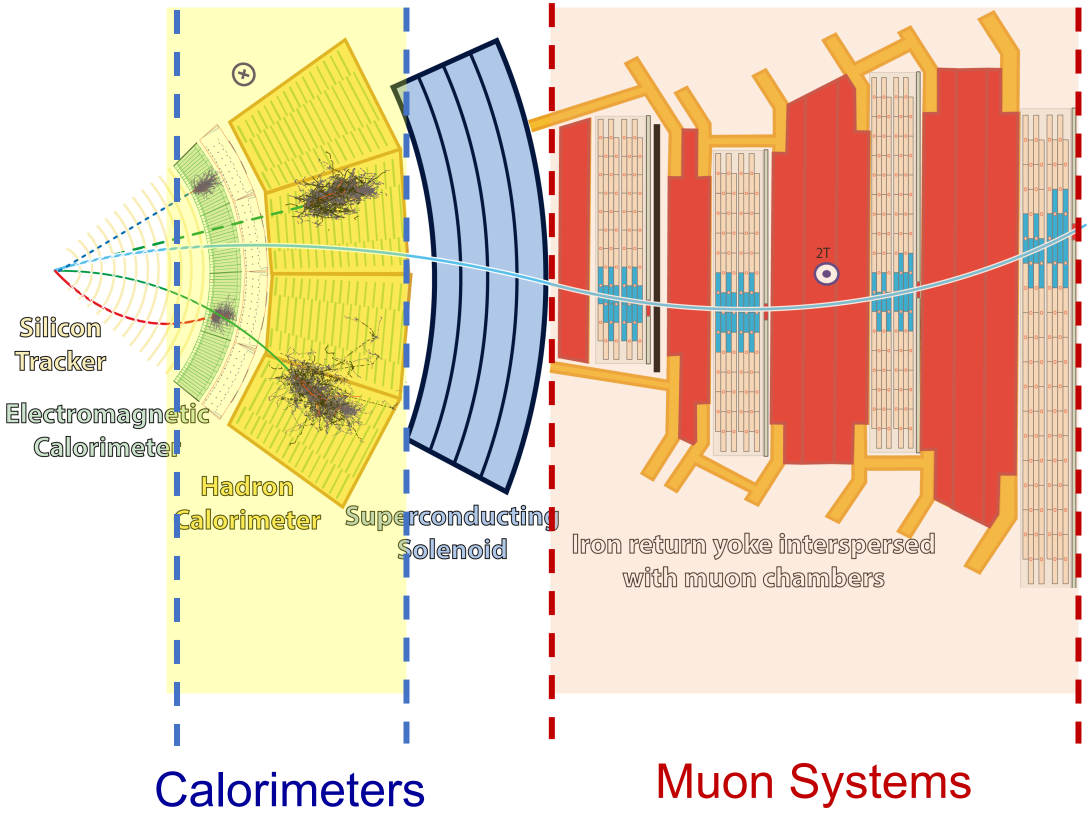
Two-level triggering:

- **Level-1 Trigger (L1T)**
  - Rate down to ~100kHz
  - Using physics criteria and only a reduced event information (no tracker, reduced ECAL resolution)
- **High Level Trigger (HLT)**
  - Rate down to ~1kHz
  - Performs a simplified event reconstruction using full RAW event

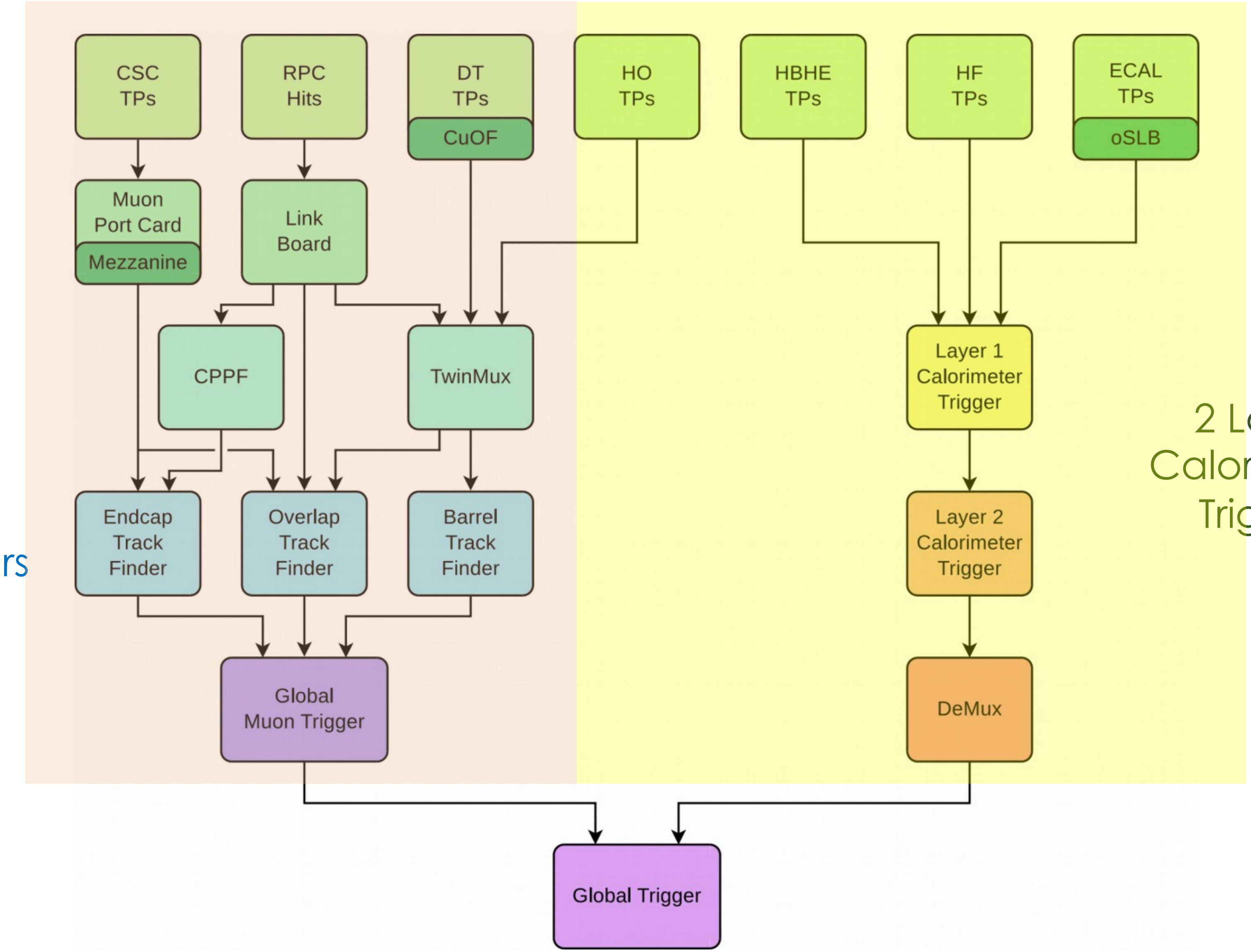


CMS Level-1 Trigger

- **Collision data are buffered locally for < 4μs**
- **Level-1 trigger receives data with coarse granularity from**
  - Calorimeters (ECAL, HCAL, HF)
  - Muon systems (CSC, DT, RPC, GEM)
- **It is implemented in hardware**
  - Mostly uses field programmable gate arrays (FPGAs)
  - Operates synchronously to the LHC clock (40 MHz)
- Detector readout possible at **<100 kHz**



Current level-1 Trigger Design



Trigger Primitives or Hits

2 Layer Calorimeter Trigger

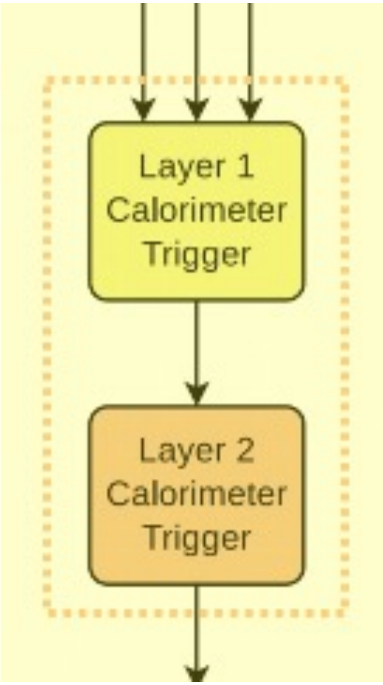
Regional Track Finders

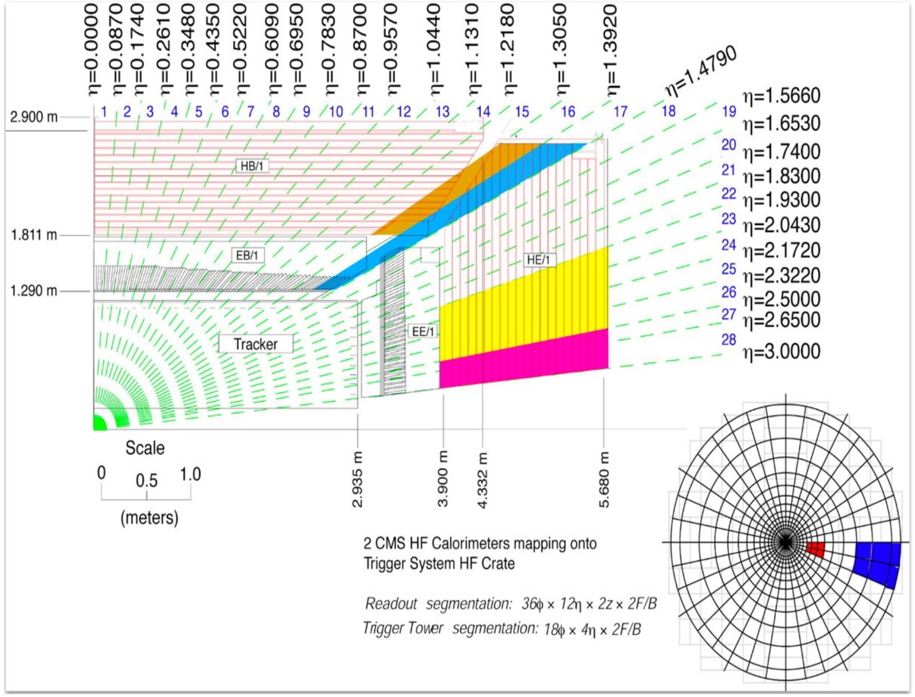
Level-1 Calorimeter Trigger

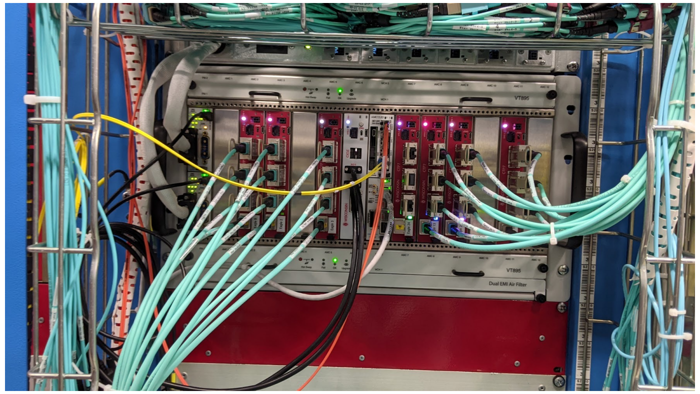
- **Two-layer calorimeter trigger**
  - Tower-level calibrations
  - Pileup subtraction
  - Independent calibrations for jets, taus, e/gamma

- **Calo Layer – 1**
  - Combines inputs from ECAL & HCAL
  - Apply calibrations

- **Calo Layer – 2**
  - Find Physics candidates: Jets, taus, & e/gamma
  - For each object, applies pileup subtraction, computes isolation, applies object-based calibrations
  - Computes global quantities: transverse energy, missing energy, etc.







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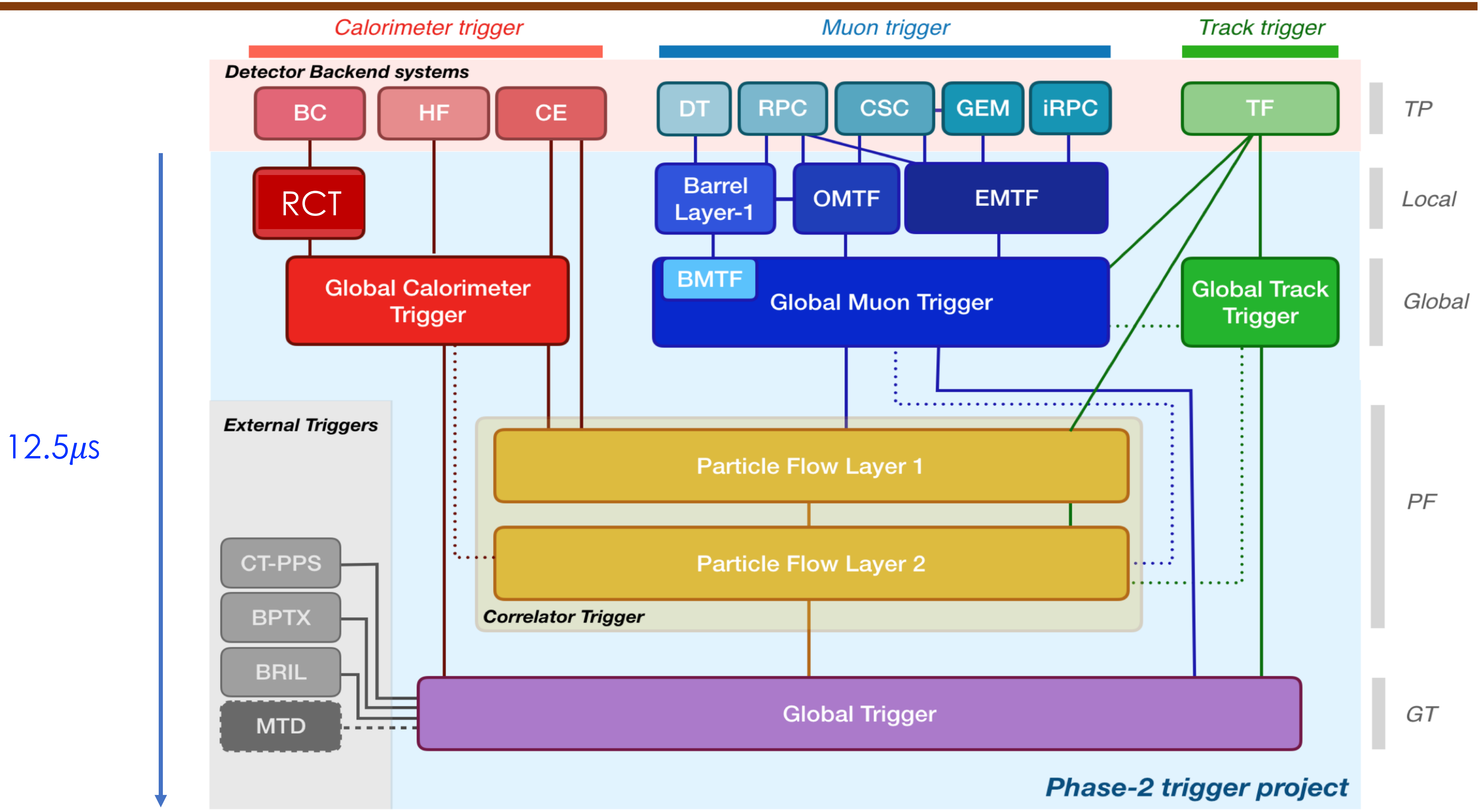
Upgrade of Level-1 Trigger

High Luminosity LHC

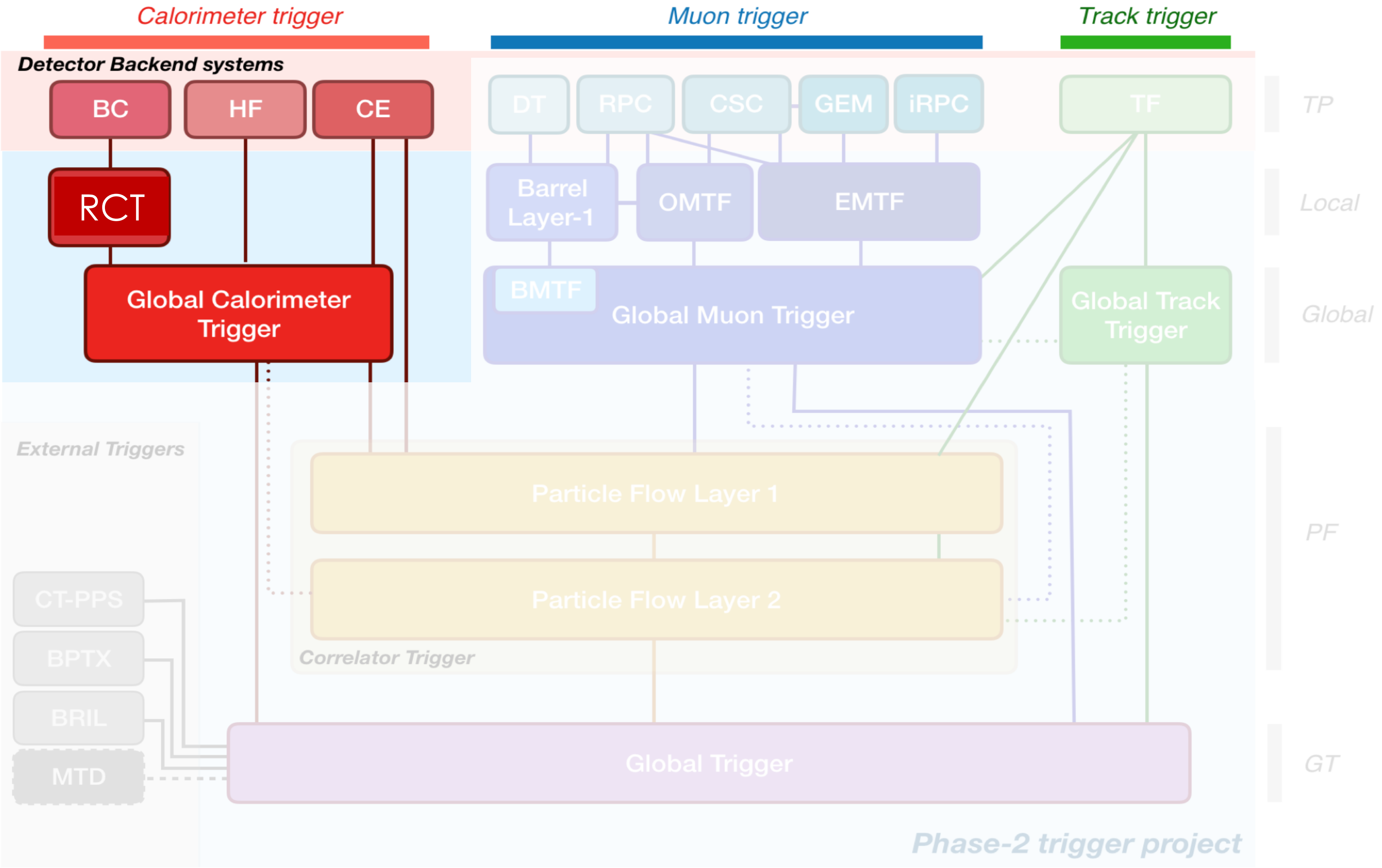
Latency: $4\mu s \Rightarrow 12.5\mu s$

Output: 100kHz ⇒ 750 kHz

Phase-2 Level-1 Trigger



Phase-2 Calorimeter Level-1 Trigger



INPUTS:

- ECAL crystals
- HCAL towers

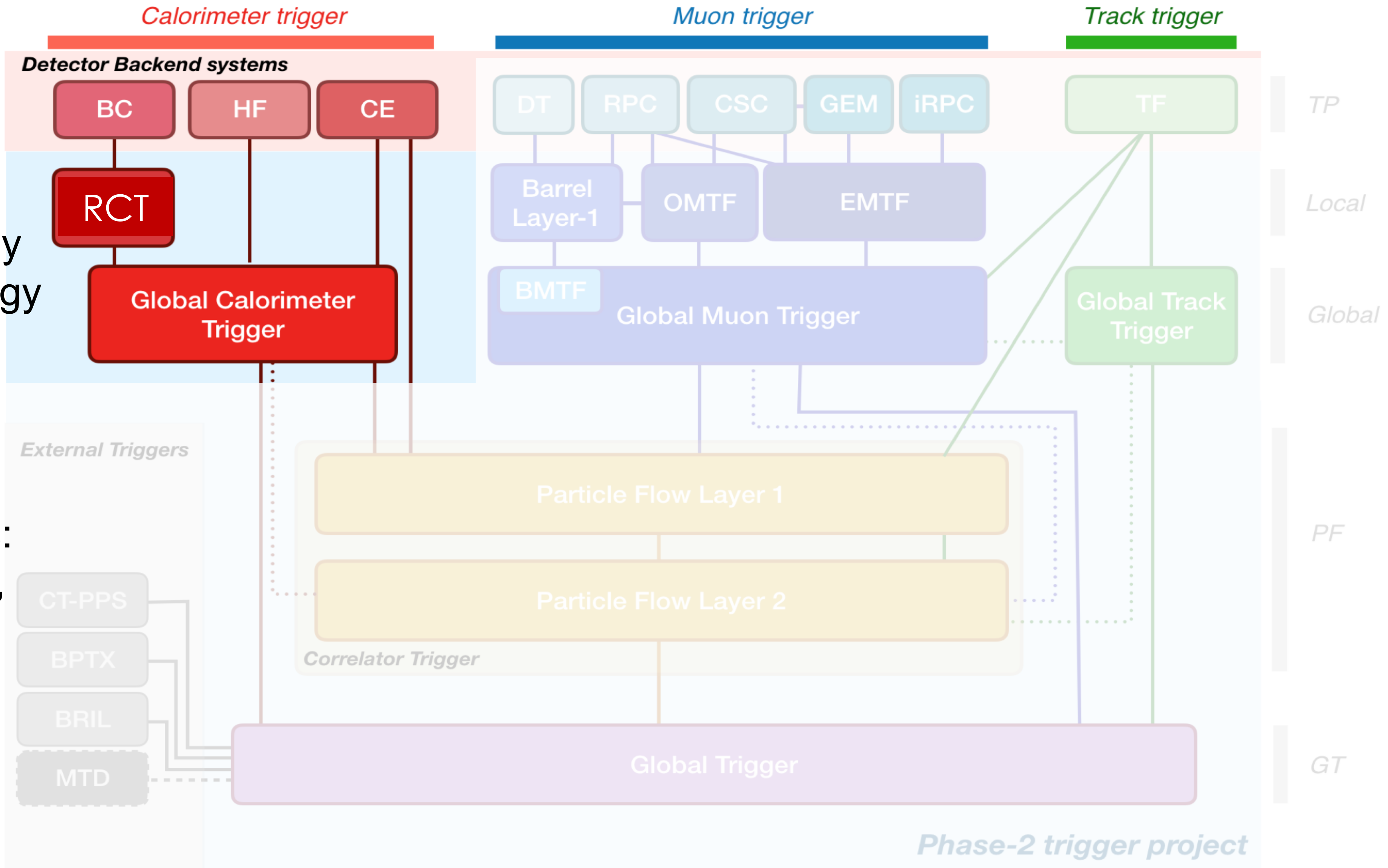
Phase-2 Calorimeter Level-1 Trigger

Outputs (RCT)

- Clustered energy
- Unclusterd energy

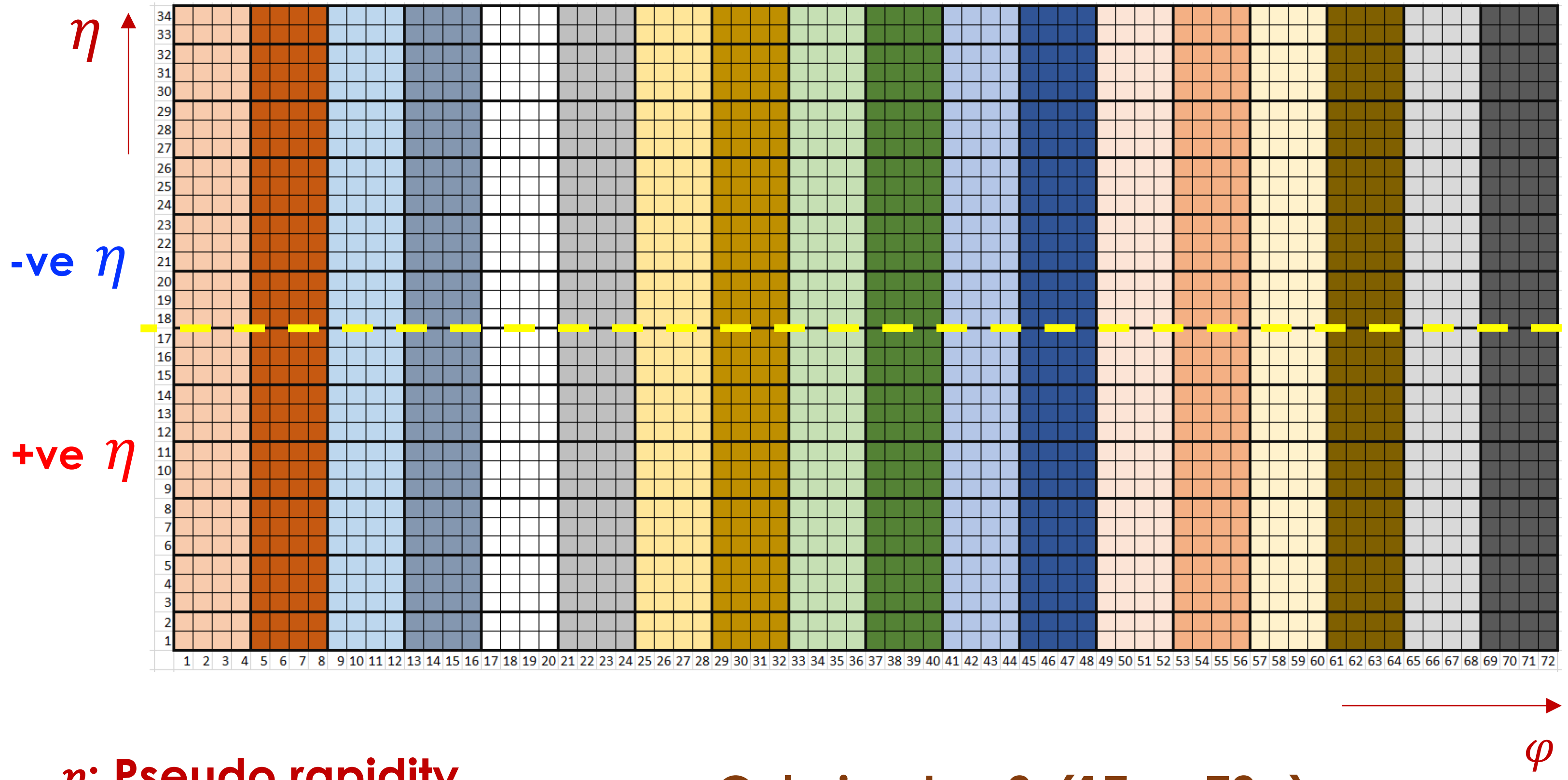
Output (GCT)

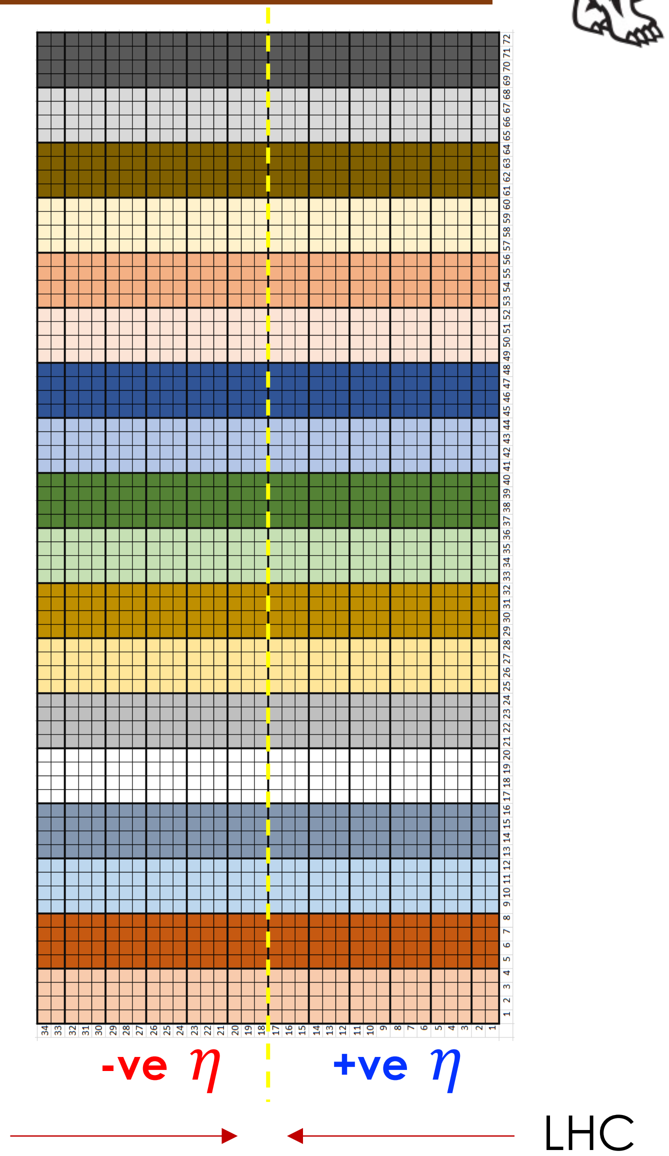
- Clusters
- Physics objects: E/gamma, taus, jets, MET
- Isolations sums



Barrel Calorimeter Granularity

Rotated 90 degrees





η: Pseudo rapidity

φ: Azimuthal angle

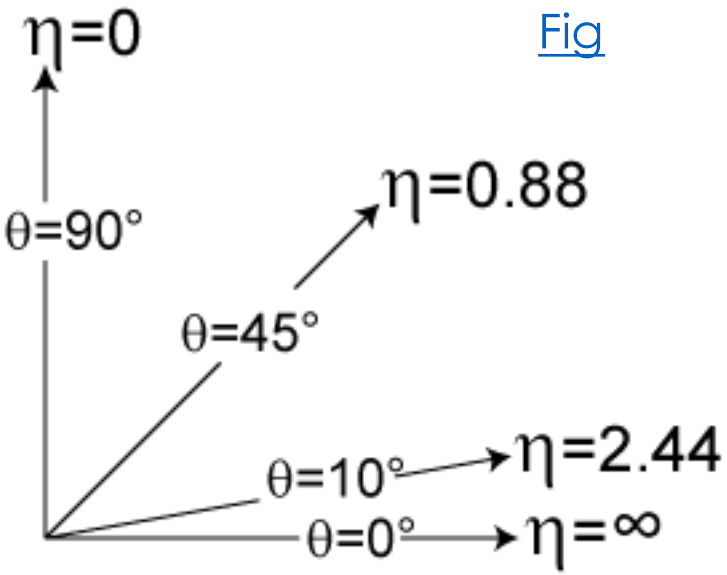
Calorimeter: 2x(17η x 72φ)

Pseudo-rapidity

Pseudo rapidity (η): Spatial coordinate describing the angle of a particle relative to the beam axis

$$\eta \equiv -\ln\left[\tan\left(\frac{\theta}{2}\right)\right]$$

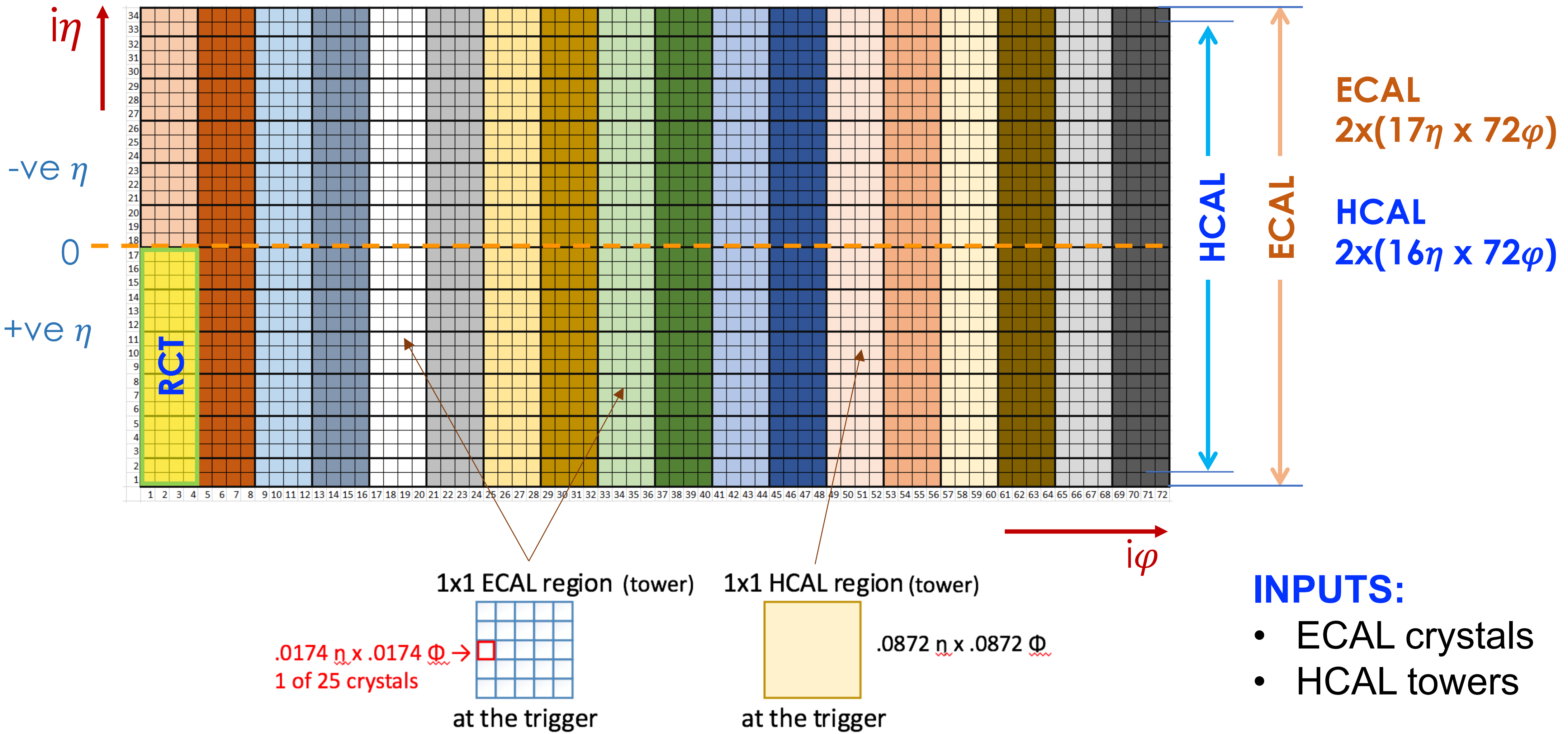
Where θ is the anlge between the particle three-momentum and the positive direction of the beam axis



Fig

Barrel Calorimeter Segmentation

36 RCT cards are needed to cover the barrel calorimeter



ECAL
$2\mathrm{x}(17\eta \times 72\varphi)$

HCAL
$2\mathrm{x}(16\eta \times 72\varphi)$

INPUTS:

- ECAL crystals
- HCAL towers

Level-1 Calo Trigger Design

- Tiled multi-layer architecture

- Regional Calorimeter Trigger (RCT): Regional Layer partitions the detector and forms regional clusters
  - No sharing between RCT cards
  - All algorithms are regional
  - Regional sums are combined at GCT

- Global Calorimeter Trigger (GCT): Global Layer stitches neighbouring clusters and forms detector-wide triggerable objects (electrons, jets, taus, ET, HT, ETmiss etc.)
  - No sharing on input data between GCT cards
  - All calculations are done in each card

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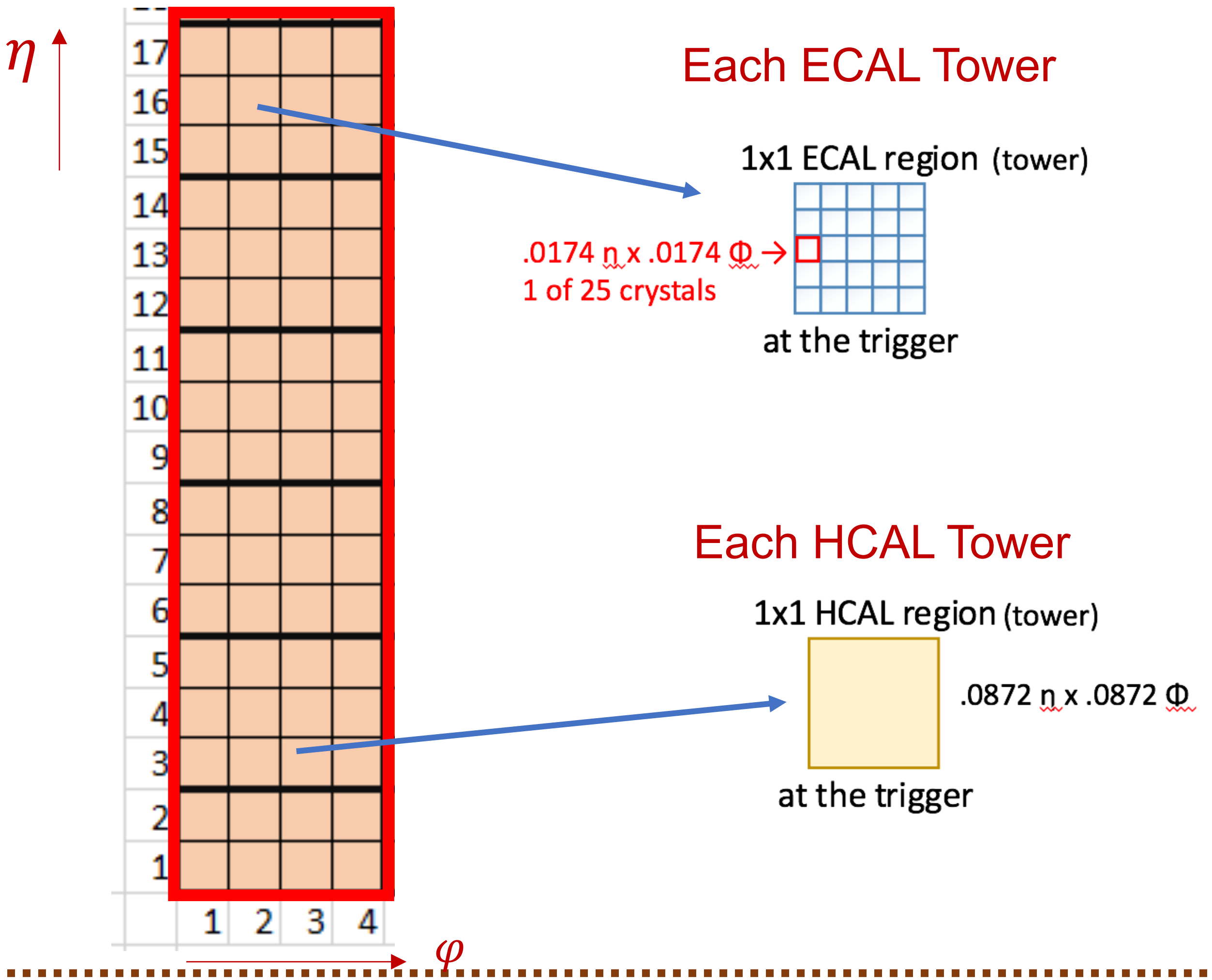
Regional Calorimenter Trigger

RCT

RCT: Overview

Each RCT card covers a geometry of 17η x 4φ and receives crystal energy as input from ECAL and tower energy from HCAL



Input
- 17x4x5x5 ECAL crystal energies
- 17x4 HCAL tower energies

ECAL crystals = 16b	10 ET + 5 timing + 1 Spike
HCAL towers = 16b	10 ET + 6 feature bits

Functionality
- Make EG towers/clusters
- ECAL + HCAL
- HoE
- …

Output
- 17x4 towers
  - Tower E_T, Cluster E_T
  - Seed Eta, Phi, Time, Isolation
  - HoE

RCT: Algorithm

Input: 17x4x5x5 ECAL crystals and 16x4 HCAL towers.

- 1-RCT card covers 17η x 4φ towers

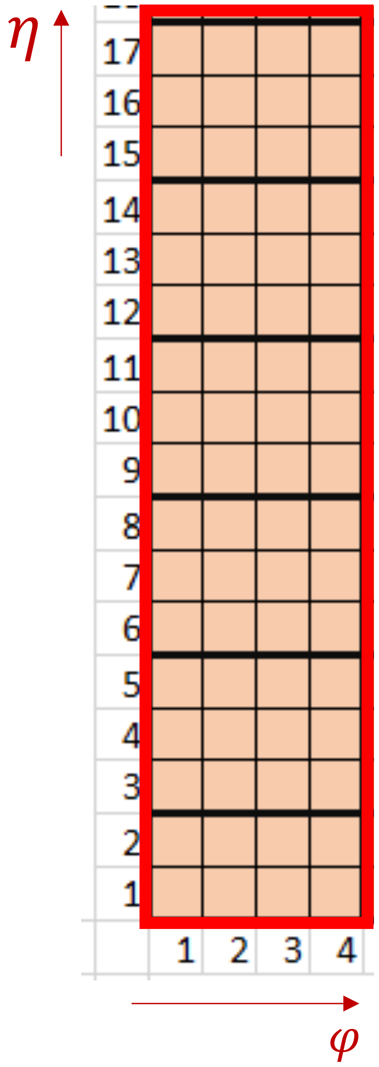
1. Divide card in regions of 3η x 4φ towers to make clusters.

2. Building clusters in 3η x 4φ region:
   - Search for seed crystal > 1 GeV
   - Make 3x5 clusters at crystal level
   - Select maximum of 5 highest ET cluster in 3η x 4φ region

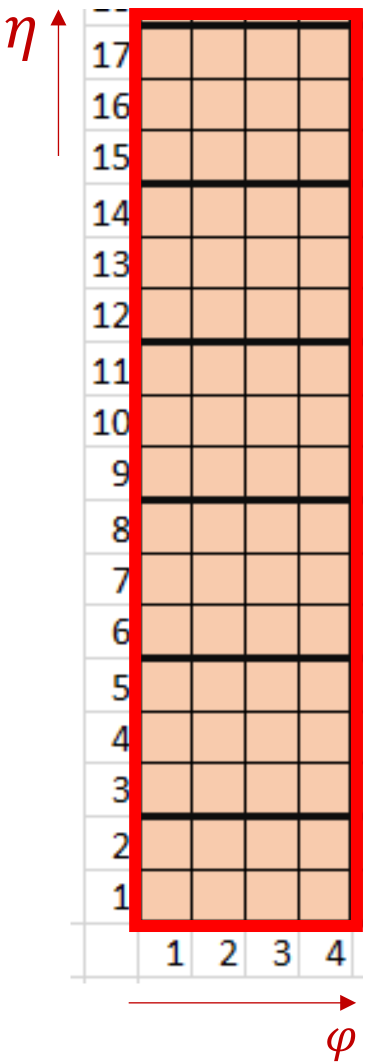
3. Move to next 3x4 towers and then do the merging around the neighbors if cluster is at the boundary of the tower

4. For 1-RCT card, there are 5 – (3η x 4φ) regions = 30 clusters
5. Sort and send a maximum of 12 highest ET clusters
6. To these 12 highest ET clusters, if there is a HCAL tower behind the ECAL tower, HCAL ET is also added to the cluster.

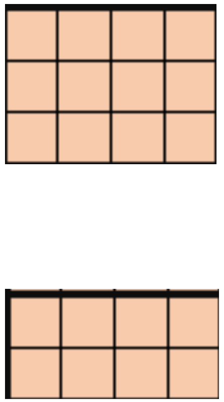
- **Output:** 12 Clusters (ECAL + HCAL)



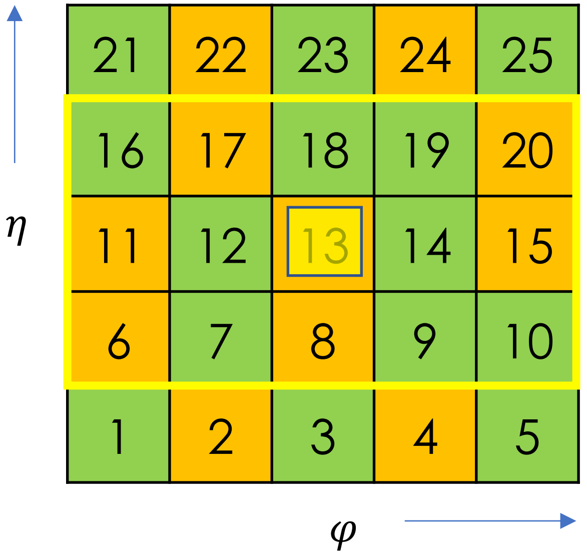
RCT: Clustering



Make 5 clusters in 1-2ηx5φ and 5-3ηx5φ regions



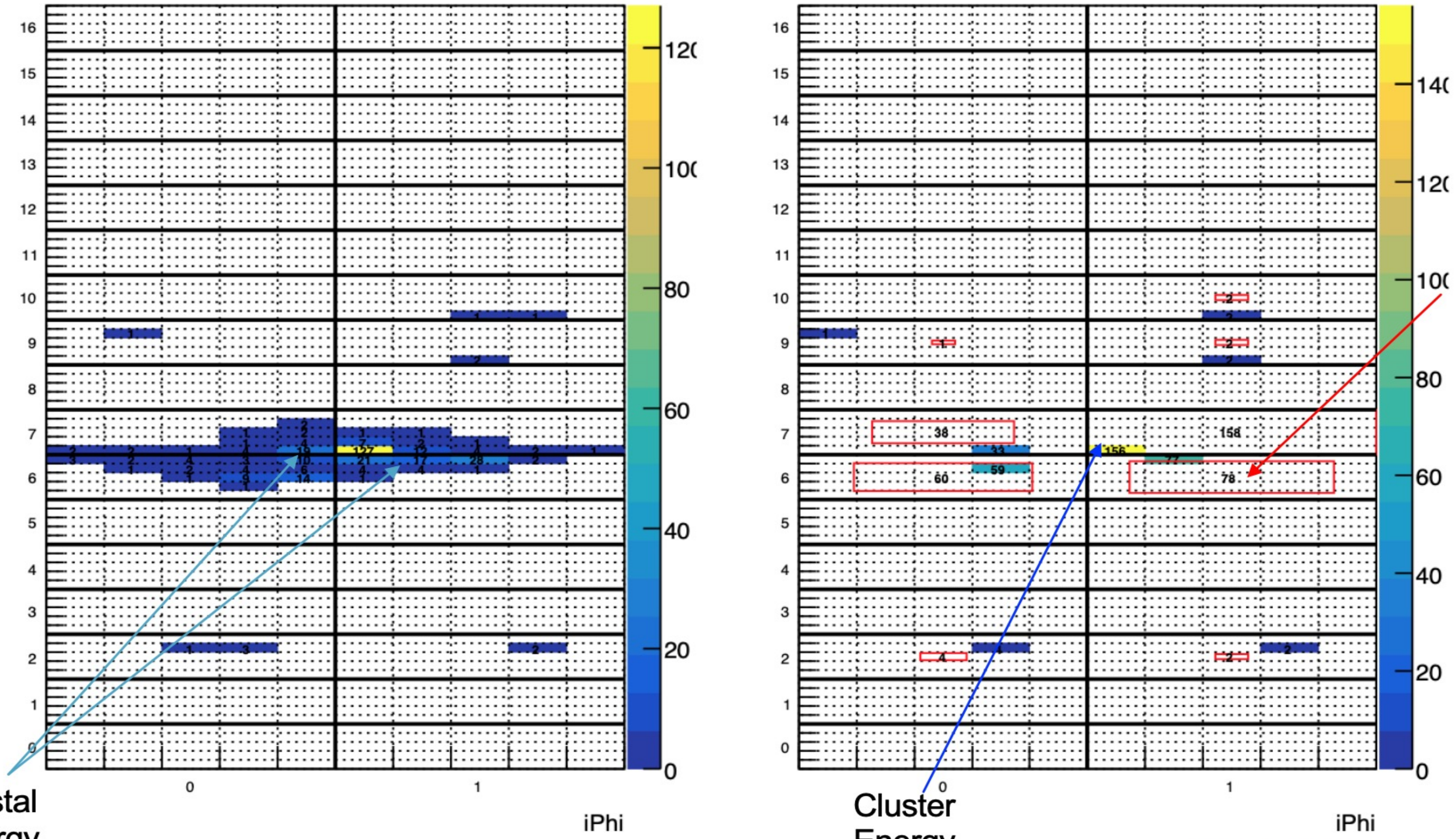
1. Building clusters in 3η x 4φ region:
   - Search for seed crystal > 1 GeV
   - Make 3x5 clusters at crystal level
   - Select maximum of 5 highest ET cluster in 3η x 4φ region



21	22	23	24	25
16	17	18	19	20
11	12	13	14	15
6	7	8	9	10
1	2	3	4	5

Look for seed crystal and then make a 3x5 cluster around it

RCT: Example



Crystal Energy

Cluster Energy

Tower Energy

July 17, 2020

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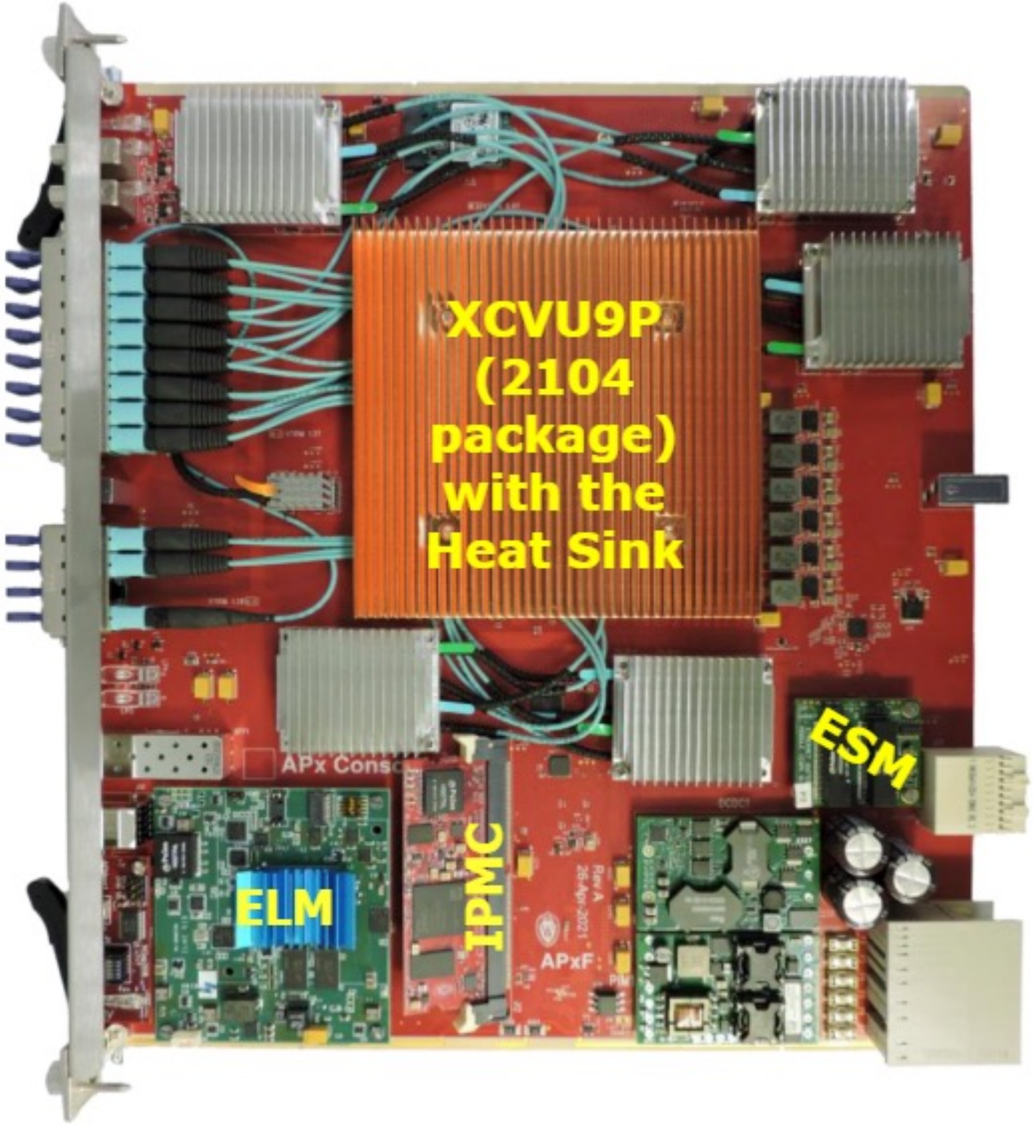
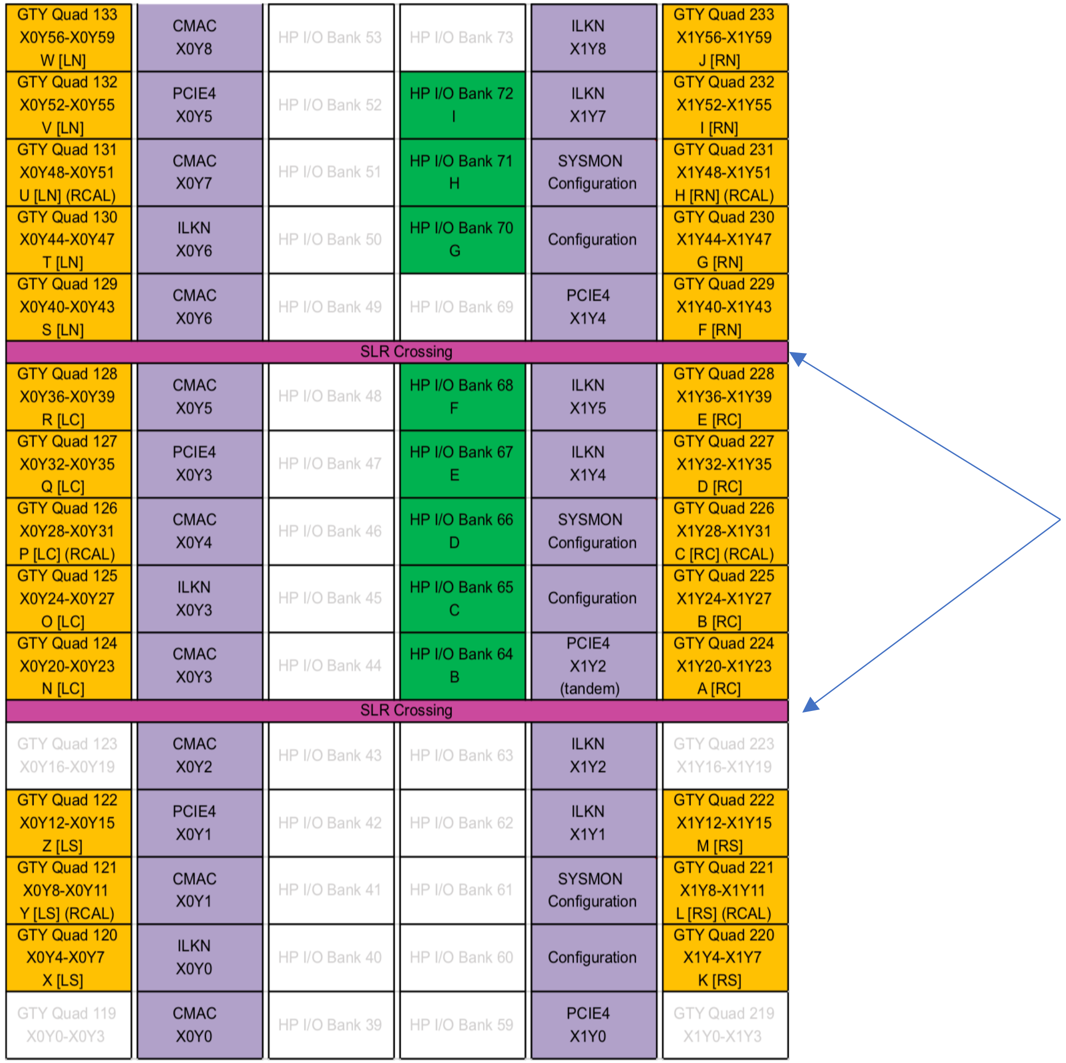
Hardware (FPGA)

Advanced Processor Demonstrator-1



Xilinx FPGA:
xcvu9p-flgc2104-1-e

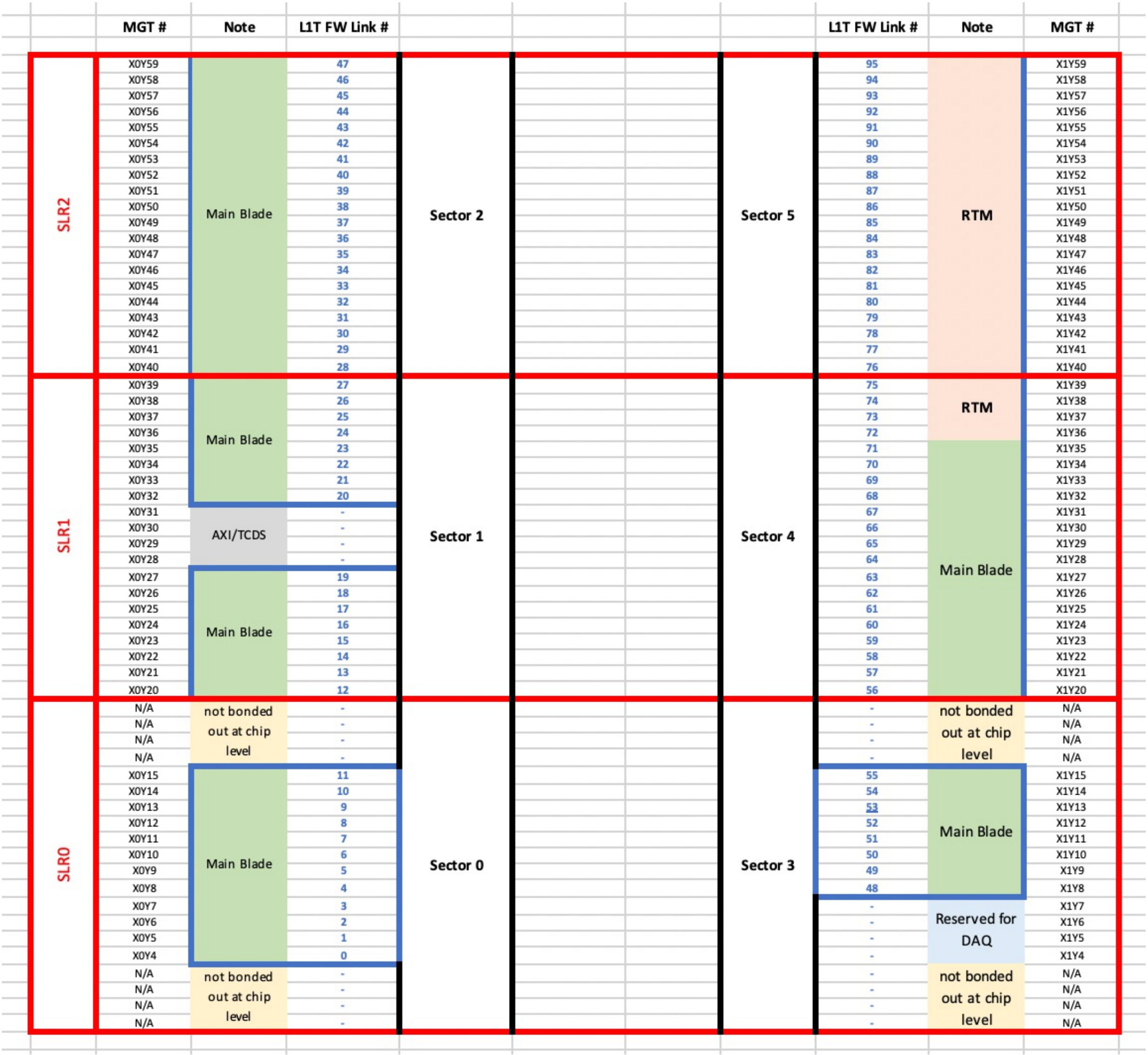
VU9P (C2104) Bank Diagram



GTY Quad 133 X0Y56-X0Y59 W [LN]	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	ILKN X1Y8	GTY Quad 233 X1Y56-X1Y59 J [RN]
GTY Quad 132 X0Y52-X0Y55 V [LN]	PCIE4 X0Y5	HP I/O Bank 52	HP I/O Bank 72 I	ILKN X1Y7	GTY Quad 232 X1Y52-X1Y55 I [RN]
GTY Quad 131 X0Y48-X0Y51 U [LN] (RCAL)	CMAC X0Y7	HP I/O Bank 51	HP I/O Bank 71 H	SYSMON Configuration	GTY Quad 231 X1Y48-X1Y51 H [RN] (RCAL)
GTY Quad 130 X0Y44-X0Y47 T [LN]	ILKN X0Y6	HP I/O Bank 50	HP I/O Bank 70 G	Configuration	GTY Quad 230 X1Y44-X1Y47 G [RN]
GTY Quad 129 X0Y40-X0Y43 S [LN]	CMAC X0Y6	HP I/O Bank 49	HP I/O Bank 69	PCIE4 X1Y4	GTY Quad 229 X1Y40-X1Y43 F [RN]
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39 R [LC]	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68 F	ILKN X1Y5	GTY Quad 228 X1Y36-X1Y39 E [RC]
GTY Quad 127 X0Y32-X0Y35 Q [LC]	PCIE4 X0Y3	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y4	GTY Quad 227 X1Y32-X1Y35 D [RC]
GTY Quad 126 X0Y28-X0Y31 P [LC] (RCAL)	CMAC X0Y4	HP I/O Bank 46	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y28-X1Y31 C [RC] (RCAL)
GTY Quad 125 X0Y24-X0Y27 O [LC]	ILKN X0Y3	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y24-X1Y27 B [RC]
GTY Quad 124 X0Y20-X0Y23 N [LC]	CMAC X0Y3	HP I/O Bank 44	HP I/O Bank 64 B	PCIE4 X1Y2 (tandem)	GTY Quad 224 X1Y20-X1Y23 A [RC]
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	ILKN X1Y2	GTY Quad 223 X1Y16-X1Y19
GTY Quad 122 X0Y12-X0Y15 Z [LS]	PCIE4 X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y1	GTY Quad 222 X1Y12-X1Y15 M [RS]
GTY Quad 121 X0Y8-X0Y11 Y [LS] (RCAL)	CMAC X0Y1	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTY Quad 221 X1Y8-X1Y11 L [RS] (RCAL)
GTY Quad 120 X0Y4-X0Y7 X [LS]	ILKN X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTY Quad 220 X1Y4-X1Y7 K [RS]
GTY Quad 119 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 39	HP I/O Bank 59	PCIE4 X1Y0	GTY Quad 219 X1Y0-X1Y3

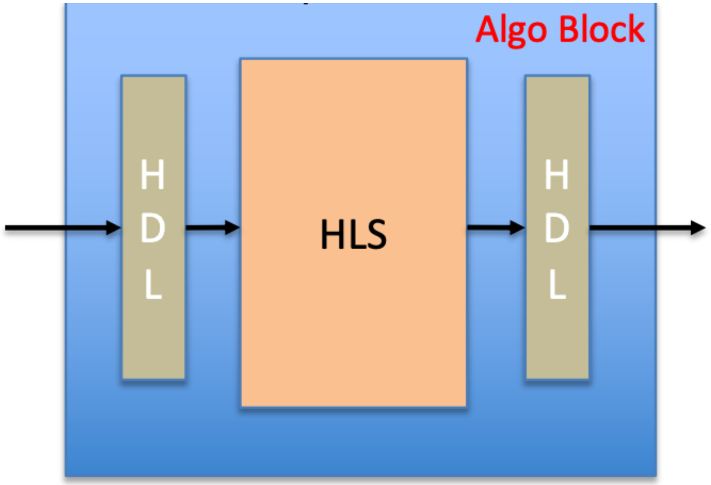
Super Logic Region (SLR) Crossing

FPGA Floor Diagram

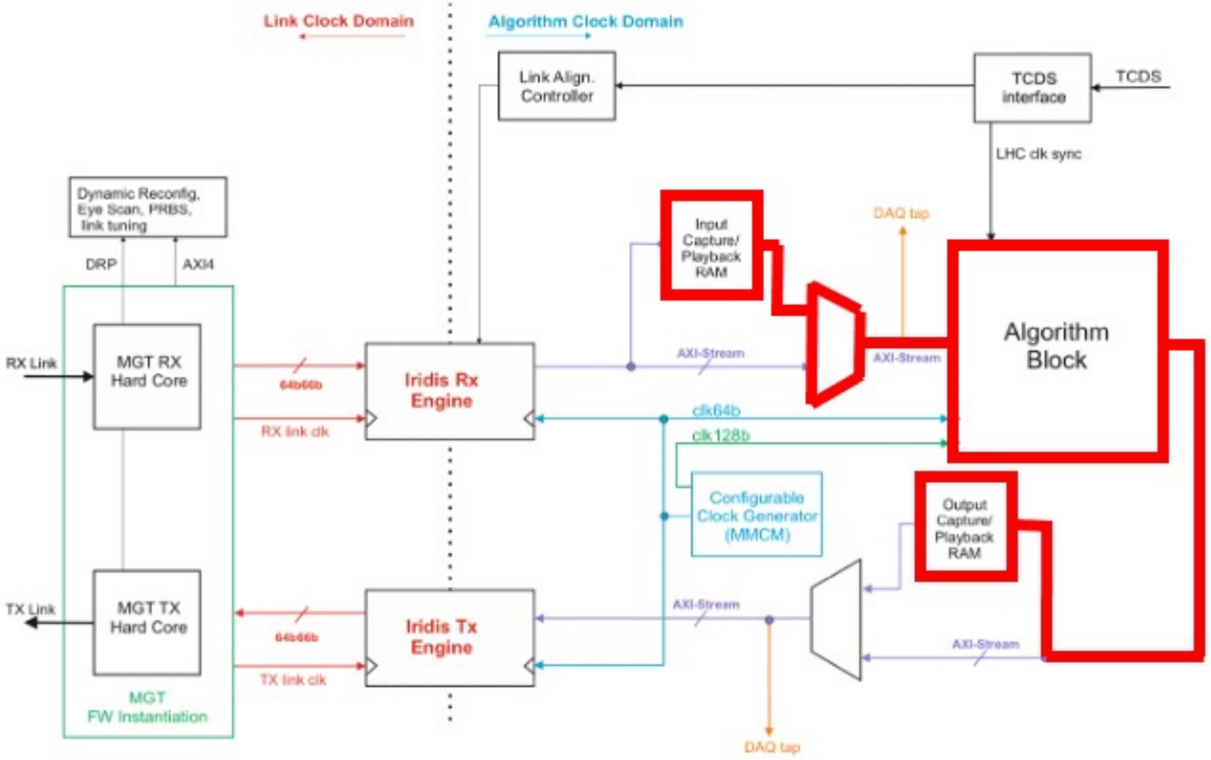


	MGT #	Note	L1T FW Link #			L1T FW Link #	Note	MGT #
SLR2	X0Y59	Main Blade	47	Sector 2	Sector 5	95	RTM	X1Y59
	X0Y58		46			94		X1Y58
	X0Y57		45			93		X1Y57
	X0Y56		44			92		X1Y56
	X0Y55		43			91		X1Y55
	X0Y54		42			90		X1Y54
	X0Y53		41			89		X1Y53
	X0Y52		40			88		X1Y52
	X0Y51		39			87		X1Y51
	X0Y50		38			86		X1Y50
	X0Y49		37			85		X1Y49
	X0Y48		36			84		X1Y48
	X0Y47		35			83		X1Y47
	X0Y46		34			82		X1Y46
	X0Y45		33			81		X1Y45
	X0Y44		32			80		X1Y44
	X0Y43		31			79		X1Y43
	X0Y42		30			78		X1Y42
	X0Y41		29			77		X1Y41
	X0Y40		28			76		X1Y40
SLR1	X0Y39	Main Blade	27	Sector 1	Sector 4	75	RTM	X1Y39
	X0Y38		26			74		X1Y38
	X0Y37		25			73		X1Y37
	X0Y36		24			72		X1Y36
	X0Y35		23			71	Main Blade	X1Y35
	X0Y34		22			70		X1Y34
	X0Y33		21			69		X1Y33
	X0Y32		20			68		X1Y32
	X0Y31	AXI/TCDS	-			67		X1Y31
	X0Y30		-			66		X1Y30
	X0Y29		-			65		X1Y29
	X0Y28		-			64		X1Y28
	X0Y27	Main Blade	19			63		X1Y27
	X0Y26		18			62		X1Y26
	X0Y25		17			61		X1Y25
	X0Y24		16			60		X1Y24
	X0Y23		15			59		X1Y23
	X0Y22		14			58		X1Y22
	X0Y21		13			57		X1Y21
	X0Y20		12			56		X1Y20
SLR0	N/A	not bonded out at chip level	-	Sector 0	Sector 3	-	not bonded out at chip level	N/A
	N/A		-			-		N/A
	N/A		-			-		N/A
	N/A		-			-		N/A
	X0Y15	Main Blade	11			55	Main Blade	X1Y15
	X0Y14		10			54		X1Y14
	X0Y13		9			53		X1Y13
	X0Y12		8			52		X1Y12
	X0Y11		7			51		X1Y11
	X0Y10		6			50		X1Y10
	X0Y9		5			49		X1Y9
	X0Y8		4			48		X1Y8
	X0Y7		3			-	Reserved for DAQ	X1Y7
	X0Y6		2			-		X1Y6
	X0Y5		1			-		X1Y5
	X0Y4		0			-		X1Y4
	N/A	not bonded out at chip level	-			-	not bonded out at chip level	N/A
	N/A		-			-		N/A
	N/A		-			-		N/A
	N/A		-			-		N/A

Some more information



APx – Firmware Shell



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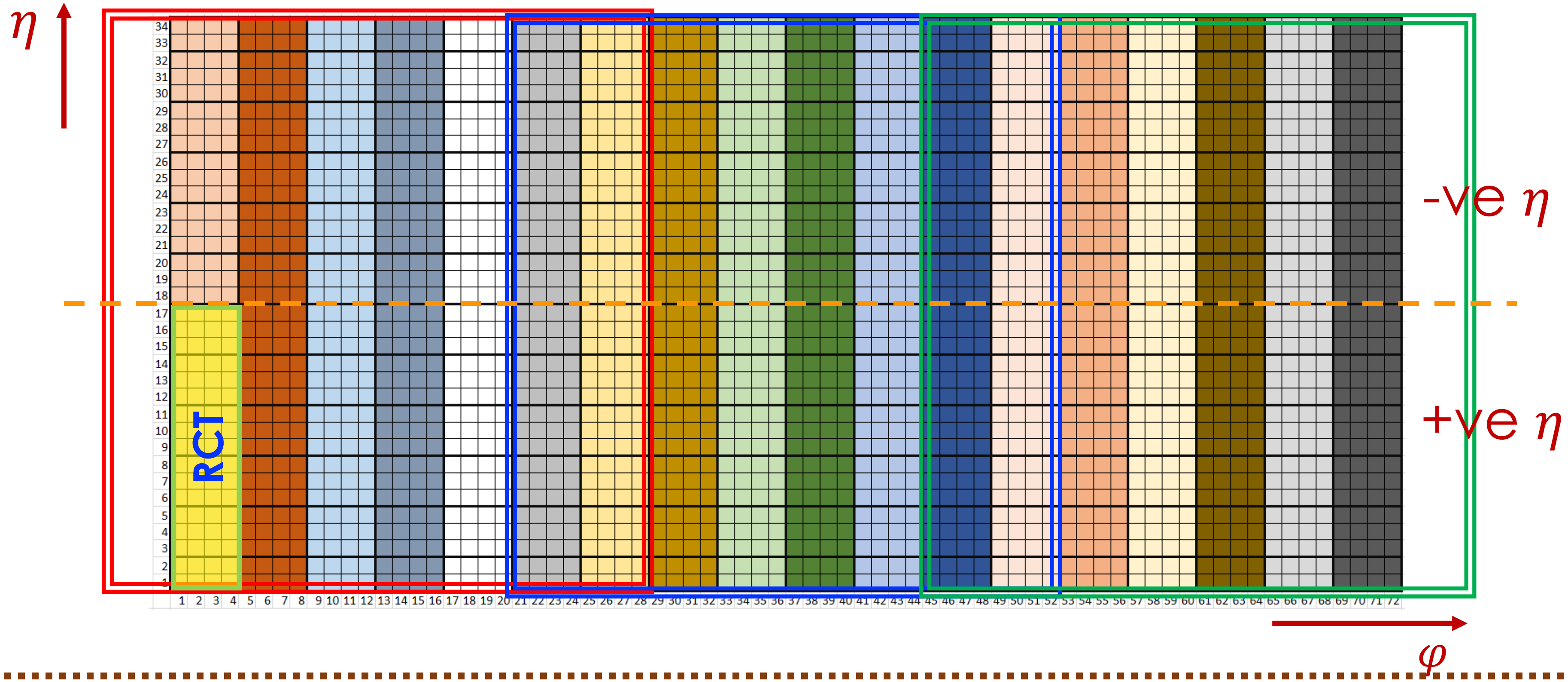
Global Calorimenter Trigger

GCT

Barrel GCT

- Each GCT takes input from 6 unique RCT cards and 2 neighbouring cards in each phi
- 1 GCT card: (1 + 6 + 1) x 2 = 16 RCT regions

1 GCT card: 16 RCT cards: (in each eta half): 6 RCT + 1 (left boundary) + 1 (right boundary)



Barrel GCT

Barrel GCT receives input from RCT

- Stitch together RCT regions in eta and phi direction
- Sends clustered energy post stitching to Correlator layer 1
- Make Physics objects – Egamma, Jets, Tau, MET (Ex, Ey), and pass onto Global Trigger

Separate projects are built for each step to produce different RTL's that will be merged to together to make one built file with help from our engineers.

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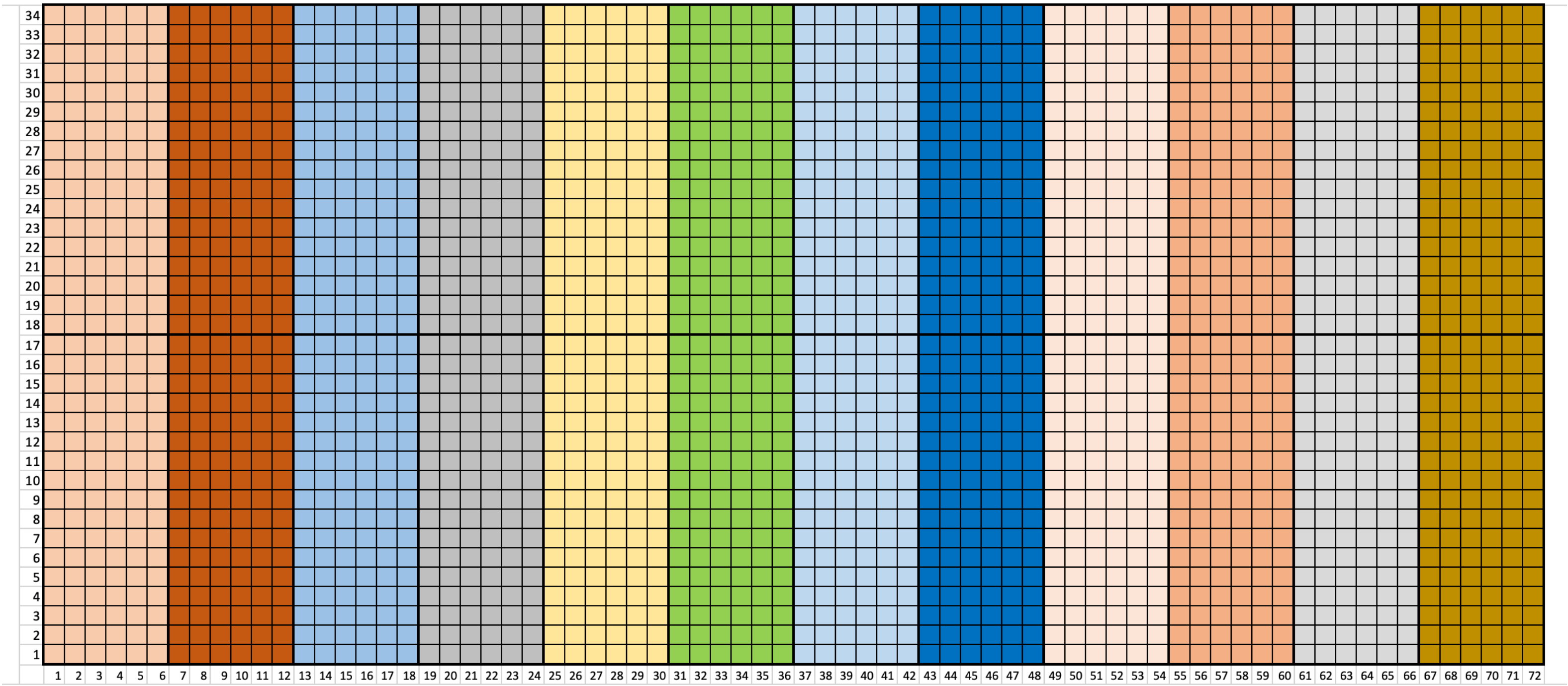
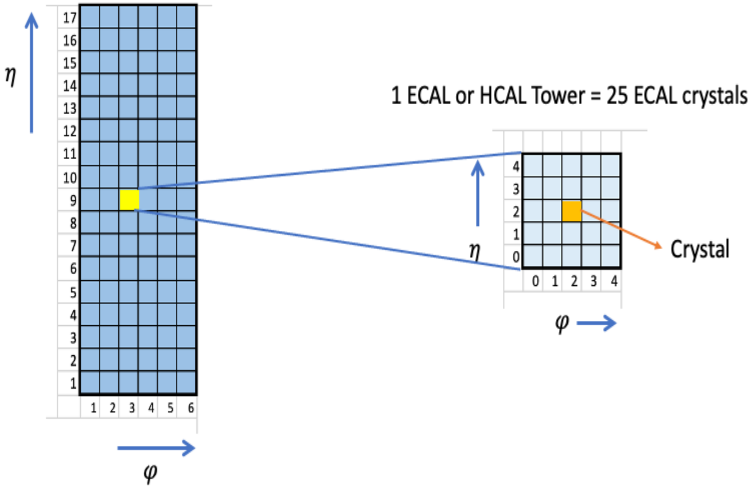
Project

Project: Re-designing RCT

- Write Regional Calorimeter Trigger Algorithm with a segmentation of calorimeter and make a bit file (steps to make bit file to be discussed tomorrow)
- New RCT: 17η x 6φ (instead of 17η x 4φ)
- Total of 24 RCT cards needed instead of 36





More tomorrow!

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Questions?

Acknowledgement

Lectures are compiled using content from Xilinx’s public pages/examples or different user guides

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Additional material

Assignment submission

- Where to submit:
  - https://pages.hep.wisc.edu/~varuns/assignments/TAC-HEP/
- Use your login machine credentials
- Submit one file per week
- Try to submit by following week's Tuesday

Correct Time

From 03.28.2023 onwards

- Tuesdays: 9:00-10:00 CT / 10:00-11:00 ET / 16:00-17:00 CET
- Wednesday: 11:00-12:00 CT / 12:00-13:00 ET / 18:00-19:00 CET

Jargons

- **ICs - Integrated chip:** assembly of hundreds of millions of transistors on a minor chip
- **PCB:** Printed Circuit Board
- **LUT - Look Up Table aka 'logic'** - generic functions on small bitwidth inputs. Combine many to build the algorithm
- **FF - Flip Flops** - control the flow of data with the clock pulse. Used to build the pipeline and achieve high throughput
- **DSP - Digital Signal Processor** - performs multiplication and other arithmetic in the FPGA
- **BRAM - Block RAM** - hardened RAM resource. More efficient memories than using LUTs for more than a few elements
- **PCIe or PCI-E - Peripheral Component Interconnect Express**: is a serial expansion bus standard for connecting a computer to one or more peripheral devices
- **InfiniBand** is a computer networking communications standard used in high-performance computing that features very high throughput and very low latency
- **HLS -** High Level Synthesis - compiler for C, C++, SystemC into FPGA IP cores
- **DRCs -** Design Rule Checks
- **HDL** - Hardware Description Language - low level language for describing circuits
- **RTL** - Register Transfer Level - the very low level description of the function and connection of logic gates
- **FIFO** – First In First Out memory
- **Latency** - time between starting processing and receiving the result
  - Measured in clock cycles or seconds
- **II - Initiation Interval** - time from accepting first input to accepting next input

Assignment Week-3

- Use target device: **xc7k160tfbg484-2**
- Clock period of 10ns

1. Execute the code (lec5Ex2.tcl) using CLI (slide-25) and compare the results with GUI results for C-Simulation, C-Synthesis

2. Vary following parameters for two cases: high and very high values and compare with 1 for both CLI and GUI
    - Variable: "samples"
    - Variable: "N"

3. Run example lec3Ex2a

Assignment Week-4

1. Do a matrix multiplication of two 1-dimensional arrays – A[N]*B[N], where N > 5
   a) Report synthesis results without any pragma directives
   b) Add as many pragma directives possible
      i. Report any conflicts (if reported in logs) between two pragmas

2. Compare the analysis perspective (Performance) for different case shared today
3. For Array_partitioning, instead of using complete, use block and cyclic with different factors

Assignment Week-5

1. Do exercise mention on slide-24
2. A matrix multiplication using two for loops and compare results for pragma loop_flatten & unroll
3. Write a simple program doing arithmetic operations(+, -, *, /, %) between two variable use of arbitrary precision to compare results between stand c/c++ data types and using ap_(u)int<N>
4. Write a program using an array with N(=10/15/20) elements and then restructure the code with a struct having N-data member. Compare the results of two programs