Traineeships in Advanced Computing for High Energy Physics (TAC-HEP)

GPU & FPGA module training: Part-2

<u>Week-3</u>: Hands-on with vivado_hls, output review

Lecture-5: April 4th 2023





Varun Sharma

University of Wisconsin – Madison, USA





FPGA and its architecture

- Registor/Flip-Flops, LUTs/Logic Cells, DSP, BRAMs
- Clock Frequency, Latency
- Extracting control logic & Implementing I/O ports
- Parallelism in FPGA
 - Scheduling, Pipelining, DataFlow
- Vivado HLS
 - Introduction, Setup

Today:

- Vivado HLS hands-on with an examples:
 - Using GUI, CLI
- Review output reports (C-Sim, C-Synthesis)

Reminder: Steps to follow



- Step-1: Creating a New Project/Opening an existing project
- Step-2: Validating the C-source code
- Step-3: High Level Synthesis
- Step-4: RTL Verification
- Step-5: IP Creation



Creating project





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Target Device: xc7k160tfbg484-2

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Selecting device

Tue 05:08 •

Device Selection Dialog

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Target Device: xc7k160tfbg484-2

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Vivado H

🏊 Vivado HLS 2020.1 👻

Select: 🚸 Parts

Filter

Boards

2.Family: Kintex®-7

4.Package: fbg484

5.Speed Grade: -2

6.Temp Grade: All

3.Sub-Family: Kintex-7

C-Simulation





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👙 Activities 🛛 👌 Vivado HLS 2020.1 👻	Tue 05:10 ●		•) () -
Vivado HLS 20	1 - lec5Ex1 (/nfs_scratch/varuns/tac-hep-fpga/lec5Ex1)		×
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lec5Ex1			

Pre-synthesis validation: Correct implementation of C-program for required functionality

Validated using a test bench

Launch Debugger: Compiles the C code & opens the debug perspective

Build Only: C code compiles, but the simulation does not run

Clean Build: Remove any existing executable and object files from the project before compiling the code.

C-Simulation





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On-going...



Finished...

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C-simulation output



lecoext.c

Test Bench
 lec5Ex1_out_ref.dat
 lec5Ex1_test.c

🔻 🛵 solution1

👻 🎕 constraints

% directives.tcl

🌿 script.tcl

🔻 🔁 csim

🔻 🔁 build

📄 apcc.log

🗟 csim.exe

🗋 csim.mk

lec5Ex1_out_ref.dat

lec5Ex1_out.dat

📄 Makefile.rules

🞾 run_sim.tcl

🧐 sim. sh

🕨 🗁 obj

🔻 🗁 report

📄 lec5Ex1_csim.log

csim/build is the primary location for all files related to the Csimulation

- Any files read by the test bench are copied to this folder
- The C executable file csim.exe is created and run in this folder
- Any files written by the test bench are created in this folder
 - Build Only option: exe file is not executed

Folder csim/report contains a log file of the C simulation

Next: execute synthesis

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<u>F</u> ile Edit Project <u>S</u> olution <u>W</u> indo	w Help	File Edit Project Solution Window Help	
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		Vivado HLS Synthesis	쪱

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C-Synthesis

Tue 05:35 •

Vivado HLS 2020.1 - lec5Ex1 (/nfs_scratch/varuns/tac-hep-fpga/lec5Ex1)

🚸 Activities 🛛 👔 Vivado HLS 2020.1 👻



Tue 05:32 •

April 4, 2023

Vivado HLS 2020.1 - lec5Ex1 (/nfs_scratch/varuns/tac-hep-fpga/lec5Ex1)



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C-Synthesis: On-going





Within GUI, some messages may contain links to enhanced information Clicking them provides more details on why message was issues and possible resolution

/ivado HLS Console /opt/Xilinx/Vivado/2020.1/bin/vivado hls /nfs scratch/varuns/tac-hep-fpga/lec5Ex1/solution1/cs INFO: [HLS 200-10] Running '/opt/Xilinx/Vivado/2020.1/bin/unwrapped/lnx64.o/vivado hls' INFO: [HLS 200-10] For user 'varuns' on host 'cmstrigger02.hep.wisc.edu' (Linux x86 64 version INFO: [HLS 200-10] On os "CentOS Linux release 7.9.2009 (Core)" INFO: [HLS 200-10] In directory '/nfs scratch/varuns/tac-hep-fpga' Sourcing Tcl script '/nfs scratch/varuns/tac-hep-fpga/lec5Ex1/solution1/csynth.tcl' INFO: [HLS 200-10] Opening project '/nfs scratch/varuns/tac-hep-fpga/lec5Ex1'. INFO: [HLS 200-10] Adding design file 'TAC-HEP-FPGA-HLS/lec5Ex1.c' to the project INFO: [HLS 200-10] Adding test bench file 'TAC-HEP-FPGA-HLS/lec5Ex1 out ref.dat' to the project INFO: [HLS 200-10] Adding test bench file 'TAC-HEP-FPGA-HLS/lec5Ex1 test.c' to the project INFO: [HLS 200-10] Opening solution '/nfs scratch/varuns/tac-hep-fpga/lec5Ex1/solution1'. INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns. INFO: [HLS 200-10] Setting target device to 'xc7k160t-fbg484-2' INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns. INFO: [SCHED 204-61] Option 'relax ii for timing' is enabled, will increase II to preserve clo-INFO: [HLS 200-10] Analyzing design file 'TAC-HEP-FPGA-HLS/lec5Ex1.c' ... INFO: [HLS 200-111] Finished Linking Time (s): cpu = 00:00:13 ; elapsed = 00:00:13 . Memory (MI INFO: [HLS 200-111] Finished Checking Pragmas Time (s): cpu = 00:00:13 ; elapsed = 00:00:13 . I INFO: [HLS 200-10] Starting code transformations ... INFO: [HLS 200-111] Finished Standard Transforms Time (s): cpu = 00:00:15 ; elapsed = 00:00:15 INFO: [HLS 200-10] Checking synthesizability ... INFO: [HLS 200-111] Finished Checking Synthesizability Time (s): cpu = 00:00:15 ; elapsed = 00 INFO: [HLS 200-111] Finished Pre-synthesis Time (s): cpu = 00:00:15 ; elapsed = 00:00:15 . Mem INFO: [HLS 200-472] Inferring partial write operation for 'arr' (TAC-HEP-FPGA-HLS/<u>lec5Ex1.c:17</u> INFO: [HLS 200-472] Inferring partial write operation for 'arr' (TAC-HEP-FPGA-HLS/lec5Ex1.c:20

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C-Synthesis: On-going

Eg.: lec5Ex1



Message: SCHED 204-61 × Within GUI, some mest Message: SCHED 204-61 Clicking them provide indicates the final performance achieved by the PIPELINE directive, esolution when issued at the end of the pipeline process. **/ivado HLS Console** /opt/Xilinx/Vivado/202 Explanation INF0: [HLS 200-10] Run INFO: [HLS 200-10] For INFO: [HLS 200-10] On When the PIPELINE directive is used on a loop or function, Vivado HLS INFO: [HLS 200-10] In seeks to pipeline the loop/function with the specified Initiation Sourcing Tcl script '/ Interval (II) using option -II. The II is the number of clock cycles INFO: [HLS 200-10] Ope between reading new input values. The fastest possible design has INFO: [HLS 200-10] Add II=1: it reads new inputs every clock cycle. If no II is specified, an INFO: [HLS 200-10] Add INFO: [HLS 200-10] Add II=1 is assumed. INF0: [HLS 200-10] Ope INFO: [SYN 201-201] Se This message specifies the required II (Target), the actual II INFO: [HLS 200-10] Set achieved (Final) and the latency (DEPTH) of the final pipeline. INF0: [SYN 201-201] Se INFO: [SCHED 204-61] | Solution INFO: [HLS 200-10] Ana INFO: [HLS 200-111] Fi INFO: [HLS 200-111] Fi If the Final II does not satisfy the requirements, refer to messages INFO: [HLS 200-10] Sta SCHED 204-68 or SCHED 204-69 issued before the previous occurrence of INFO: [HLS 200-111] Fi this message. INF0: [HLS 200-10] Che INFO: [HLS 200-111] Fi INF0: [HLS 200-111] Fi OK INFO: [HLS 200-472] Ir INFO: [HLS 200-472] In

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C-Synthesis: On-going



VIVADO HES CONSOLE INFO: [HLS 200-10] Synthesizing 'lec5Ex1' ... INF0: [HLS 200-10] -----INFO: [HLS 200-42] -- Implementing module 'lec5Ex1' INFO: [HLS 200-10] -----INFO: [SCHED 204-11] Starting scheduling ... INFO: [SCHED 204-11] Finished scheduling. INFO: [HLS 200-111] Elapsed time: 14.91 seconds; current allocated memory: 138.261 MB. INFO: [BIND 205-100] Starting micro-architecture generation ... INFO: [BIND 205-101] Performing variable lifetime analysis. INFO: [BIND 205-101] Exploring resource sharing. INFO: [BIND 205-101] Binding ... INFO: [BIND 205-100] Finished micro-architecture generation. INFO: [HLS 200-111] Elapsed time: 0.09 seconds; current allocated memory: 138.433 MB. INF0: [HLS 200-10] ----INFO: [HLS 200-10] -- Generating RTL for module 'lec5Ex1' INF0: [HLS 200-10] --INFO: [RTGEN 206-500] Setting interface mode on port 'lec5Ex1/y' to 'ap vld'. INFO: [RTGEN 206-500] Setting interface mode on port 'lec5Ex1/c' to 'ap memory'. INFO: [RTGEN 206-500] Setting interface mode on port 'lec5Ex1/x' to 'ap none'. INFO: [RTGEN 206-500] Setting interface mode on function 'lec5Ex1' to 'ap ctrl hs'. INFO: [RTGEN 206-100] Finished creating RTL model for 'lec5Ex1'. INFO: [HLS 200-111] Elapsed time: 0.14 seconds; current allocated memory: 138.727 MB. INFO: [HLS 200-790] **** Loop Constraint Status: All loop constraints were satisfied. INF0: [HLS 200-789] **** Estimated Fmax: 122.67 MHz INFO: [RTMG 210-278] Implementing memory 'lec5Ex1 arr ram (RAM)' using distributed RAMs with p

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C-Synthesis: Finished

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	Vivado HLS 2020.1 - lec5Ex1 (/nfs_scratch/varuns/tac-hep-fpga/lec5Ex1) ×
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■ lec5Ex1_out_ref.dat	21 data = arr[1];
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👻 🗁 syn	INFO: [BIND 205-101] Finished micro-architecture generation.
🔻 🗁 report	INFO: [HLS 200-111] Elapsed time: 0.09 seconds; current allocated memory: 138.433 MB.
lec5Ex1_csynth.rpt	INFO: [HLS 200-10] Generating RTL for module 'lec5Ex1'
▼	INFO: [HLS 200-10]
c lec5Ex1_arr.h	INFO: <u>IRIGEN 206-500</u> Setting interface mode on port 'lec5Ex1/y' to 'ap_vld'. INFO: [RTGEN 206-500] Setting interface mode on port 'lec5Ex1/c' to 'ab memory'.
C lec5Ex1.cpp	INFO: <u>[RTGEN 206-500]</u> Setting interface mode on port 'lec5Ex1/x' to 'ap_none'.
	INFO: <u>[RTGEN 206-100]</u> Finished creating RTL model for 'lec5Ex1'.
🔻 🗁 verilog	INFO: [HLS 200-111] Elapsed time: 0.14 seconds; current allocated memory: 138.727 MB.
lec5Ex1_arr_ram.dat	INFO: [HLS 200-789] **** Estimated Fmax: 122.67 MHz
RT lec5Ex1_arr.v	INFO: [RTMG 210-278] Implementing memory 'lec5Ex1 arr ram (RAM)' using distributed RAMs with puter of the second s
attlec5Ex1.v	INFO: [VHDL 208-304] Generating VHDL RTL for lec5Ex1.
▼	INFO: [VLOG 209-307] Generating Verilog RTL for lec5Ex1.
Rt lec5Ex1_arr.vhd	Finished C synthesis.
RT lec5Ex1.vhd	
	· · · · · · · · · · · · · · · · · · ·





Synthesis Report for 'lec5Ex1'

General Information

	Date:	Tue Apr 4 05:32:18 2023
	Version:	2020.1 (Build 2897737 on Wed May 27 20:21:37 MDT 2020)
	Project:	lec5Ex1
	Solution:	solution1
	Product family:	kintex7
	Target device:	xc7k160t-fbg484-2
I	Performance Es	stimates
	Timing	
	Summary	
	-	
	Clock Targ	et EstimatedUncertainty
	Clock Targ ap_clk10.00	et EstimatedUncertainty ns 8.152 ns 1.25 ns
Console	Clock Targ ap_clk10.00	et EstimatedUncertainty ns 8.152 ns 1.25 ns nings EURCS 23
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🚡 Explorer ន 💌 💷 rest Bench

lec5Ex1_out_ref.dat
 lec5Ex1_test.c

- 🔻 👍 solution1
 - 🕨 🏶 constraints
 - 🕨 🗁 csim
 - 🕨 🗁 impl
 - 🔻 🗁 syn
 - 🔻 🗁 report

lec5Ex1_csynth.rpt

🔻 🗁 systemc

.c lec5Ex1_arr.h

🖻 lec5Ex1.cpp

🖻 lec5Ex1.h

🔻 🗁 verilog

📄 lec5Ex1_arr_ram.dat

- RT lec5Ex1_arr.v
- RT lec5Ex1.v

🔻 🗁 vhdl

RT lec5Ex1_arr.vhd

RT lec5Ex1.vhd

Folder syn is now available in the solution folder

report folder contains a report file for the top-level function and one for every sub-function in the design

verilog, vhdl, and systemc folders contain the output RTL files

The top-level file has the same name as the top-level function for synthesis

One RTL file for each function

Might be additional RTL files to implement sub-blocks (block RAM, pipelined multipliers, etc)

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Design Rule Checks

C-Synthesis: Review the output

🖳 Console 🧐 Errors 🙆 Warnings 🖆 DRCs 🕱								
🖸 🖻 🕀 🚼 🗹 3 DRC-Infos 🗹 0 DRC-Warnings 🗹 0 DRC-Errors 😂								
Name Details								
- • All Categories								
▼ • THROUGHPUT								
i [HLS 200-789] **** Estimated Fmax: 122.67 MHz								
i [SCHED 204-61] Option 'relax_ii_for_timing' is enabled, will increase II to pre	serve clock fre							
✓ LOOP								
i [HLS 200-790] **** Loop Constraint Status: All loop constraints were satis	fied.							
solution1 🛙								





Eg.: lec5Ex1



Synthesis Report for 'lec5Ex1'

General Information

Date: Tue Apr 4 05:32:18 2023

- Version: 2020.1 (Build 2897737 on Wed May 27 20:21:37 MDT 2020)
- Project: lec5Ex1
- Solution: solution1
- Product family: kintex7

Target device: xc7k160t-fbg484-2

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	8.152 ns	1.25 ns

Latency

Summary

Latency	(cycles)	Latency (absolute)	Interval	(cycles)	
min	max	min	max	min	max	Туре
34	34	0.340 us	0.340 us	34	34	none

General Information: Details on when the results were generated, software version used, project name, solution name, & technology details

Timing: target clock frequency, clock uncertainty, & the estimate of the fastest achievable clock frequency

Latency Summary:

•

- Reports the latency and II for this block and any sub-blocks
 instantiated in this block
- Each sub-function called at this level in the C source is an instance in this RTL block unless it was inlined
- Latency: # of CLK cycle to get output
- II: # of CLK cycle before new inputs can arrive
 - Without PIPELINE directives: Latency = II -1
 - Next input is read when the final output is written

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Latency Detail:

- Latency and II for the instances sub-functions & loops in this block
 - For sub-loops, the loop hierarchy is shown
- Min and max latency values indicate the latency to execute all iterations of the loop
 - Conditional branches might make the min and max different

- Iteration Latency: latency for a single iteration of the loop
- For variable loop latency, values can't be determined and are shown as a "?"
- Any specified target initiation interval is shown beside the actual initiation interval achieved
- The *tripcount* shows the total number of loop iterations

- Loop

	Latency	(cycles)		Initiation I	nterval		
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop	33	33	3	-	-	11	no

Latency Summary

Detail

N/A

Instance

Latency	(cycles)	Latency (absolute)	Interval	(cycles)	
min	max	min	max	min	max	Туре
34	34 34		0.340 us	34	34non	



Eg.: lec5Ex1

Latency Detail:

- Latency and II for the instances sub-functions & loops in this block
 - For sub-loops, the loop hierarchy is shown
- Min and max latency values indicate the latency to execute all iterations of the loop
 - Conditional branches might make the min and max different

- No sub-blocks in this design.: Expanding the Instance section shows no sub-modules in the hierarchy
- All the delay is due to the RTL logic synthesized from the loop named "Loop"
- Total latency is one clock cycle greater than the loop latency
 - Requires one clock cycle to enter and exit the loop (in this case, the design finishes when the loop finishes, so there is no exit cycle)



Eg.: lec5Ex1

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Latency

- Summarv

	'				
Latency	(cycles)	Latency	(absolute)	Interval	(cycle
min	max	min	max	min	max
34	34	0.340 us	s 0.340 us	34	

🖃 Detail

N/A

Instance

Loop

	Latency	(cycles)		Initiation I	nterval		
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop	33	33	3	-	-	11	no

Type 34none





Utilization Estimates

Summary

Detail

Instance
 DSP48E

Memory

Expression
 Multiplexer

Register

FIFO

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	3	0	86	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	64	6	0
Multiplexer	-	-	-	91	-
Register	-	-	111	-	-
Total	0	3	175	183	0
Available	650	600	202800	101400	0
Utilization (%)	0	~0	~0	~0	0

Report shows the resources: LUTS, Flip-Flops, DSPs, used to implement the design

Instance: Resources used by sub-blocks instantiated at this hierarchy

- If no RTL hierarchy, no instances reported
- For any instance, detail report is presented

Memory: Resources used in implementation of memories

FIFO: Resources used in implementation of any FIFO

Expressions: Resources used by any expressions such as multipliers, adders, and comparators along with bit widths of the input ports to the expressions

Multiplexers: Resources used to implement multiplexors along with bit-widths of input ports

Registers: List of all shift registers used

synthesis

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	3	0	86	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	64	6	0
Multiplexer	-	-	-	91	-
Register	-	-	111	-	-
Total	0	3	175	183	0
Available	650	600	202800	101400	0
Utilization (%)	0	~0	~0	~0	0

The design uses 3 DSP48s, 175 flip-flops and 183LUTs.

At this stage, the area numbers are estimates

RTL synthesis might be able to perform additional

optimizations, and these figures might change after RTL

- Instance
- DSP48E
- Memory
- FIFO
- Expression
- Multiplexer
- Register

🗆 Detail

Eg.: lec5Ex1

Interface

Summary

DTID	D.:	D		c	C T
RIL Ports	Dir	Bits	Protocol	Source Object	CType
ap_clk	in	1	ap_ctrl_hs	lec5Ex1	return value
ap_rst	in	1	ap_ctrl_hs	lec5Ex1	return value
ap_start	in	1	ap_ctrl_hs	lec5Ex1	return value
ap_done	out	1	ap_ctrl_hs	lec5Ex1	return value
ap_idle	out	1	ap_ctrl_hs	lec5Ex1	return value
ap_ready	out	1	ap_ctrl_hs	lec5Ex1	return value
у	out	32	ap_vld	У	pointer
y_ap_vld	out	1	ap_vld	У	pointer
c_address0	out	4	ap_memory	c	array
c_ce0	out	1	ap_memory	c	array
c_q0	in	32	ap_memory	c	array
х	in	32	ap_none	x	scalar

Export the report (.html) using the Export Wizard

Open Analysis Perspective

Analysis Perspective

Shows how the the function arguments have been synthesized into RTL ports

The RTL port names are grouped with their protocol and source object: these are the RTL ports created when that source object is synthesized with the stated I/O protocol

The design has a clock and reset port

Synthesis has automatically added some block level control ports : ap_start, ap_done, ap_idle and ap_ready





Eg.: lec5Ex1

File Edit Project Solution Window Help

Analysis Perspective

Analysis Perspective to analyze the results

📮 🔚 🐂 🗶 🗁 🖪 🗊 🕶 🖺 🔐 🚱 🥨 梦 Debug [▲] Synthesis & Analysis lec5Ex1.c Synthesis(solut) RT lec5Ex1_arr.v RT lec5Ex1.v ☐ Resource Viewer ☎ »7 - 4 8 5 ۲ Q Q :: ۵ 8 Operation\Control Step 12 2 0 З f ▼ [+]I/O Ports Ξ read х write c(p0) read [+]Memory Ports arr(p0) write write c(p0) read [+]Expressions i_0_phi_fu_108 phi_mux sum_0_phi_fu_95 phi_mux qrp_fu_125 +icmp_ln16_fu_144 icmp data_0_phi_fu_119 phi_mux sum_fu_169 + mul_ln23_fu_163 ×. Schedule Viewer Resource Viewer

Resource view



Eg.: lec5Ex1

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Analysis Perspective







Schedule viewer

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Vivado HLS via CLI



1 open_project lec5Ex2

- 2 set_top lec5Ex1
- 3 add_files lec5Ex1.c
- 4 add_files -tb lec5Ex1_test.c
- 5 add_files -tb lec5Ex1_out_ref.dat
- 6

```
7 open_solution "solution1"
```

```
8 set_part {xc7k160tfbg484-2}
```

```
9 create_clock -period 10
```

```
10
```

```
11 #source "./lec5Ex2/solution1/directives.tcl"
```

```
12
```

```
13 csim_design
```

```
14 csynth_design
```

```
15 cosim_design
```

```
16 #export_design -format ip_catalog
```

```
17
```

```
18 # Exit Vivado HLS
```

```
19 exit
```

https://github.com/varuns23/TAC-HEP-FPGA-HLS/blob/main/lec5Ex2.tcl

Execute: vivado_hls lec5Ex2.tcl

Vivado HLS via CLI

What to expect...

[varuns@cmstrigger02 TAC-HEP-FPGA-HLS]\$ vivado_hls lec5Ex2.tcl
****** Vivado(TM) HLS - High-Level Synthesis from C, C++ and SystemC v2020.1 (64-bit) **** SW Build 2902540 on Wed May 27 19:54:35 MDT 2020 **** IP Build 2902112 on Wed May 27 22:43:36 MDT 2020 ** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.
source /opt/Xilinx/Vivado/2020.1/scripts/vivado_hls/hls.tcl -notrace INFO: [HLS 200-10] Running '/opt/Xilinx/Vivado/2020.1/bin/unwrapped/lnx64.o/vivado_hls' INFO: [HLS 200-10] For user 'varuns' on host 'cmstrigger02.hep.wisc.edu' (Linux_x86_64 version 5.4.236-1.el7.elrepo.x86_64) on Tue Apr 04 08:09:19 CDT 2023 INFO: [HLS 200-10] On os "CentOS Linux release 7.9.2009 (Core)" INFO: [HLS 200-10] In directory '/nfs_scratch/varuns/tac-hep-fpga/TAC-HEP-FPGA-HLS'
Sourcing Tcl script 'lec5Ex2.tcl' INFO: [HLS 200-10] Creating and opening project '/nfs_scratch/varuns/tac-hep-fpga/TAC-HEP-FPGA-HLS/lec5Ex2'. INFO: [HLS 200-10] Adding design file 'lec5Ex1.c' to the project INFO: [HLS 200-10] Adding test bench file 'lec5Ex1_test.c' to the project
INFO: [HLS 200-10] Adding test bench file 'lec5Ex1_out_ref.dat' to the project INFO: [HLS 200-10] Creating and opening solution '/nfs_scratch/varuns/tac-hep-fpga/TAC-HEP-FPGA-HLS/lec5Ex2/solution1'. INFO: [HLS 200-10] Setting target device to 'xc7k160t-fbg484-2' INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
<pre>INF0: [SIM 211-2] ************** CSIM start ***********************************</pre>
INFO: [HLS 200-10] For user 'varuns' on host 'cmstrigger02.hep.wisc.edu' (Linux_x86_64 version 5.4.236-1.el7.elrepo.x86_64) on Tue Apr 04 08:09:25 CDT 2023 INFO: [HLS 200-10] On os "CentOS Linux release 7.9.2009 (Core)" INFO: [HLS 200-10] In directory '/nfs_scratch/varuns/tac-hep-fpga/TAC-HEP-FPGA-HLS/lec5Ex2/solution1/csim/build' INFO: [APCC 202-3] Tmp directory is /tmp/apcc_db_varuns/318961680613765501282
Compiling(apcc) ./././/lec5Ex1.c in debug mode INFO: [HLS 200-10] Running '/opt/Xilinx/Vivado/2020.1/bin/unwrapped/lnx64.o/apcc' INFO: [HLS 200-10] For user 'varuns' on host 'cmstrigger02.hep.wisc.edu' (Linux_x86_64 version 5.4.236-1.el7.elrepo.x86_64) on Tue Apr 04 08:09:38 CDT 2023 INFO: [HLS 200-10] On os "CentOS Linux release 7.9.2009 (Core)"
INFO: [HLS 200-10] In directory '/nfs_scratch/varuns/tac-hep-fpga/TAC-HEP-FPGA-HLS/lec5Ex2/solution1/csim/build' INFO: [APCC 202-3] Tmp directory is /tmp/apcc_db_varuns/320261680613778403386 INFO: [APCC 202-1] APCC is done.

Generating csim.exe

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• Git clone: https://github.com/varuns23/TAC-HEP-FPGA-HLS.git

۵	lec4Ex1.c
۵	lec4Ex1.h
ß	lec4Ex1_out_ref.dat
۵	lec4Ex1_test.c
۵	lec5Ex1.c
۵	lec5Ex1.h
۵	lec5Ex1_out_ref.dat
ß	lec5Ex1_test.c
۵	lec5Ex2.tcl
ß	out_ref.dat



Assignment



- Use target device: xc7k160tfbg484-2
- Clock period of 10ns

1. Execute the code (lec5Ex2.tcl) using CLI (slide-25) and compare the results with GUI results for C-Simulation, C-Synthesis

2. Vary following parameters for two cases: high and very high values and compare with 1 for both CLI and GUI

- Variable: "samples"
- Variable: "N"

- Where to submit:
 - <u>https://pages.hep.wisc.edu/~varuns/assignments/TAC-HEP/</u>
- Use your login machine credentials
- Submit one file per week
 - Week-2 & 3 can be merged together
- Try to submit by next Tuesday





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Additional material

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From 03.28.2023 onwards

- Tuesdays: 9:00-10:00 CT / 10:00-11:00 ET / 16:00-17:00 CET
- Wednesday: 11:00-12:00 CT / 12:00-13:00 ET / 18:00-19:00 CET

Jargons



- ICs Integrated chip: assembly of hundreds of millions of transistors on a minor chip
- **PCB:** Printed Circuit Board
- LUT Look Up Table aka 'logic' generic functions on small bitwidth inputs. Combine many to build the algorithm
- FF Flip Flops control the flow of data with the clock pulse. Used to build the pipeline and achieve high throughput
- DSP Digital Signal Processor performs multiplication and other arithmetic in the FPGA
- BRAM Block RAM hardened RAM resource. More efficient memories than using LUTs for more than a few elements
- PCIe or PCI-E Peripheral Component Interconnect Express: is a serial expansion bus standard for connecting a computer to one or more peripheral devices
- InfiniBand is a computer networking communications standard used in high-performance computing that features very high throughput and very low latency
- HLS High Level Synthesis compiler for C, C++, SystemC into FPGA IP cores
- DRCs Design Rule Checks
- HDL Hardware Description Language low level language for describing circuits
- RTL Register Transfer Level the very low level description of the function and connection of logic gates
- FIFO First In First Out memory
- Latency time between starting processing and receiving the result
 - Measured in clock cycles or seconds
- II Initiation Interval time from accepting first input to accepting next input



All set for hands-on



Everytime

<u>Summary</u>

- ssh varuns@cmstrigger02-via-login -L5901:localhost:5901
 - Or whatever: 1 display number
 - Sometimes you may need to run vncserver localhost -geometry 1024x768 again to start new vnc server
- Connect to VNC server (remote desktop) client
- Open terminal
- Source /opt/Xilinx/Vivado/2020.1/settings64.sh
- vivado_hls

		localhost:59	1 (cmstrigger02.hep.wisc.edu:1 (varuns)) - VNC View	rer
🌵 Activi	ties 🛛 👌 Vivado HLS 20	020.1 👻	Tue 07:14 ●	ti) () →
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Homework: You are able to connect and bring this screen Let me know in case of any issue

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