Traineeships in Advanced Computing for High Energy Physics (TAC-HEP)

FPGA module training

Week-5

Lecture-10: 27/02/2025

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Content

- Vivado/Vitis HLS Setup
  - First project

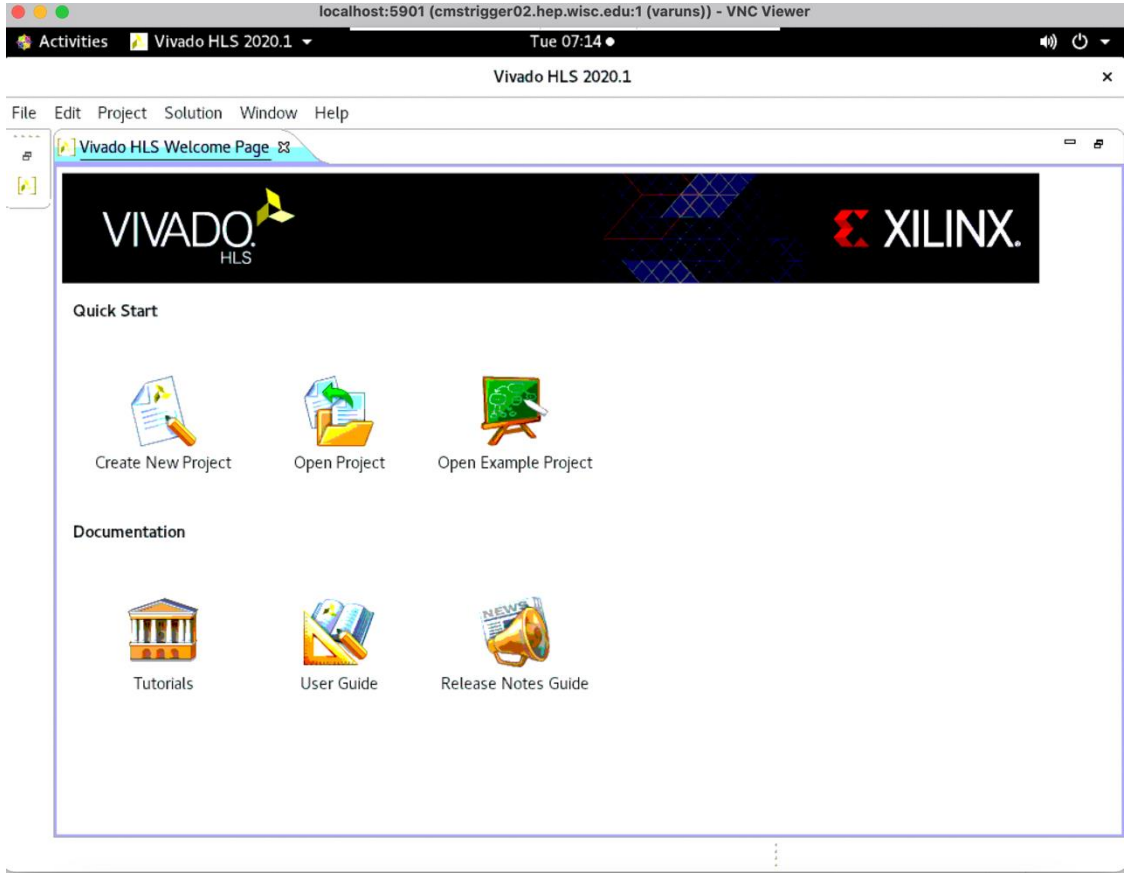
Reminder: HLS Setup

- ssh <username>@cmstrigger02-via-login -L5901:localhost:5901
  - Or whatever ***:1*** display number
  - Sometimes you may need to run vncserver -localhost -geometry 1024x768 again to start new vnc server

- **Connect to VNC server (remote desktop) client**
- **Open terminal**
  - source /opt/Xilinx/Vivado/2020.1/settings64.sh
  - cd /scratch/`whoami`
  - vivado_hls

OR

  - Source /opt/Xilinx/Vitis/2020.1/settings64.sh
  - Cd /scratch/`whoami`
  - vitis_hls



Steps to IP Creation

- **Step-1: Creating a New Project/Opening an existing project**
- **Step-2: Validating the C-source code**
- **Step-3: High Level Synthesis**
- **Step-4: RTL Verification**
- **Step-5: IP Creation**

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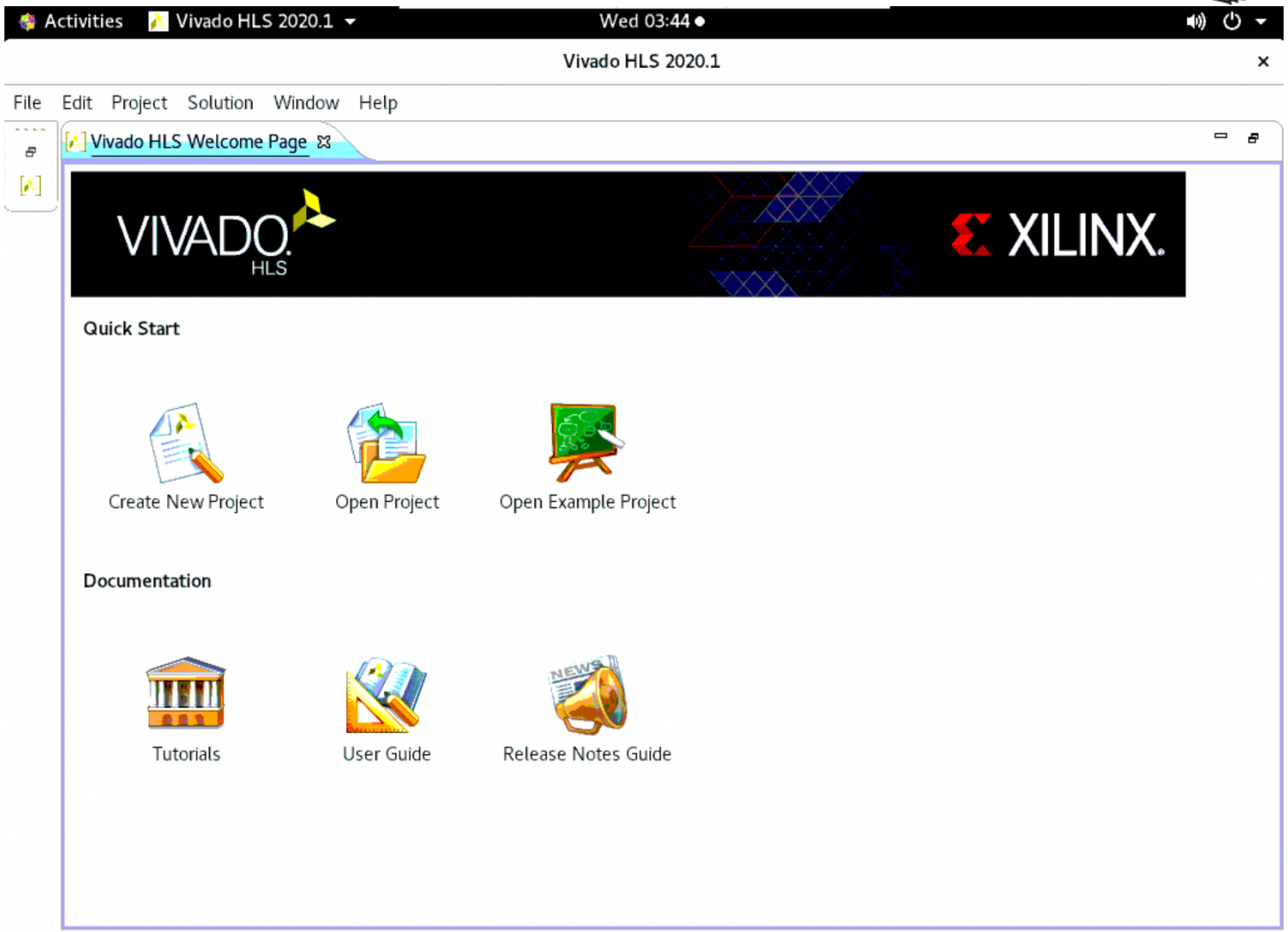
Create a new project

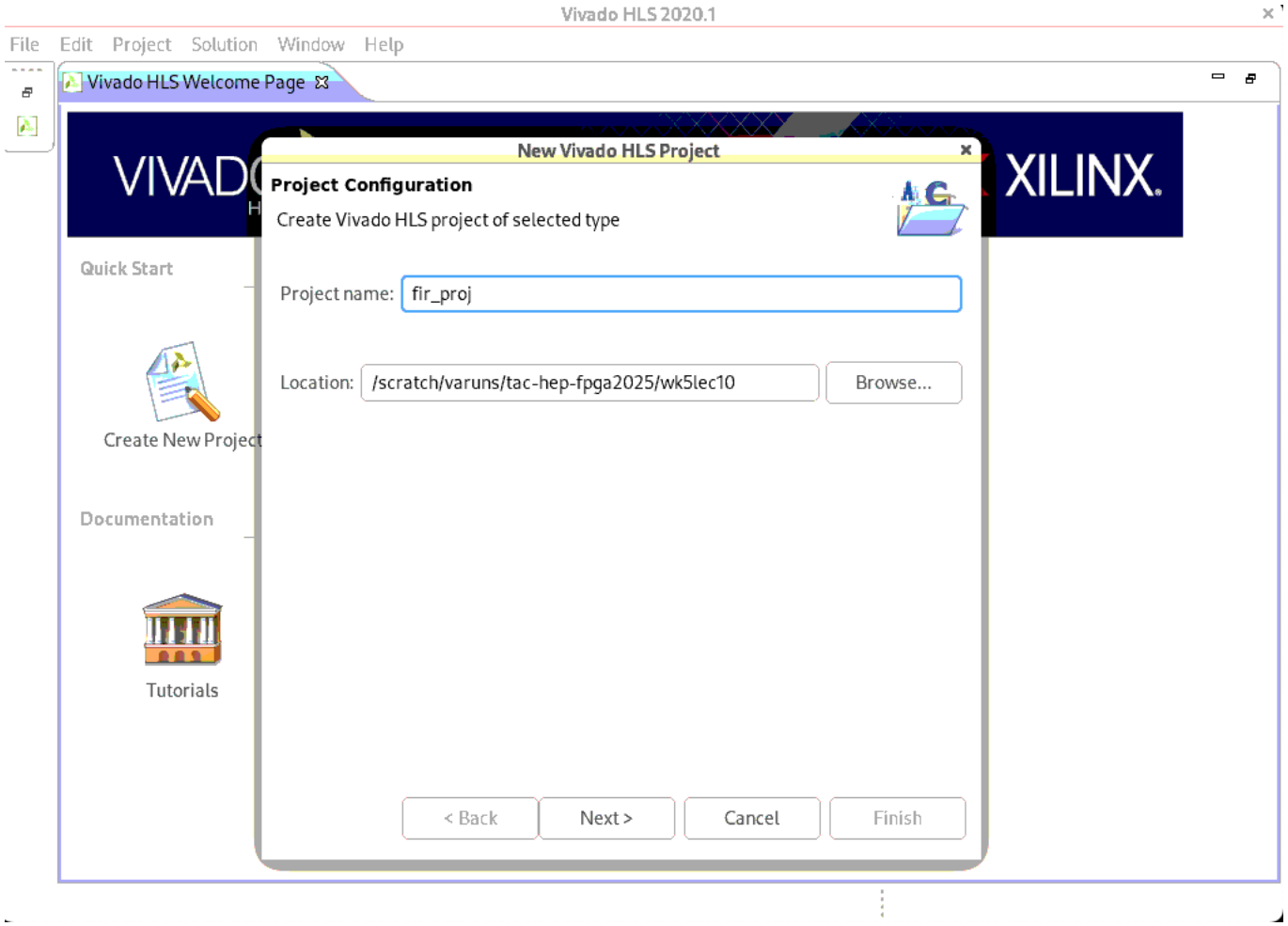
Using Vivado HLS



- Once connected to **cmstrigger02**
- Source the settings
- Go to **/scratch/`whoami`** directory
- Execute ***vivado_hls***

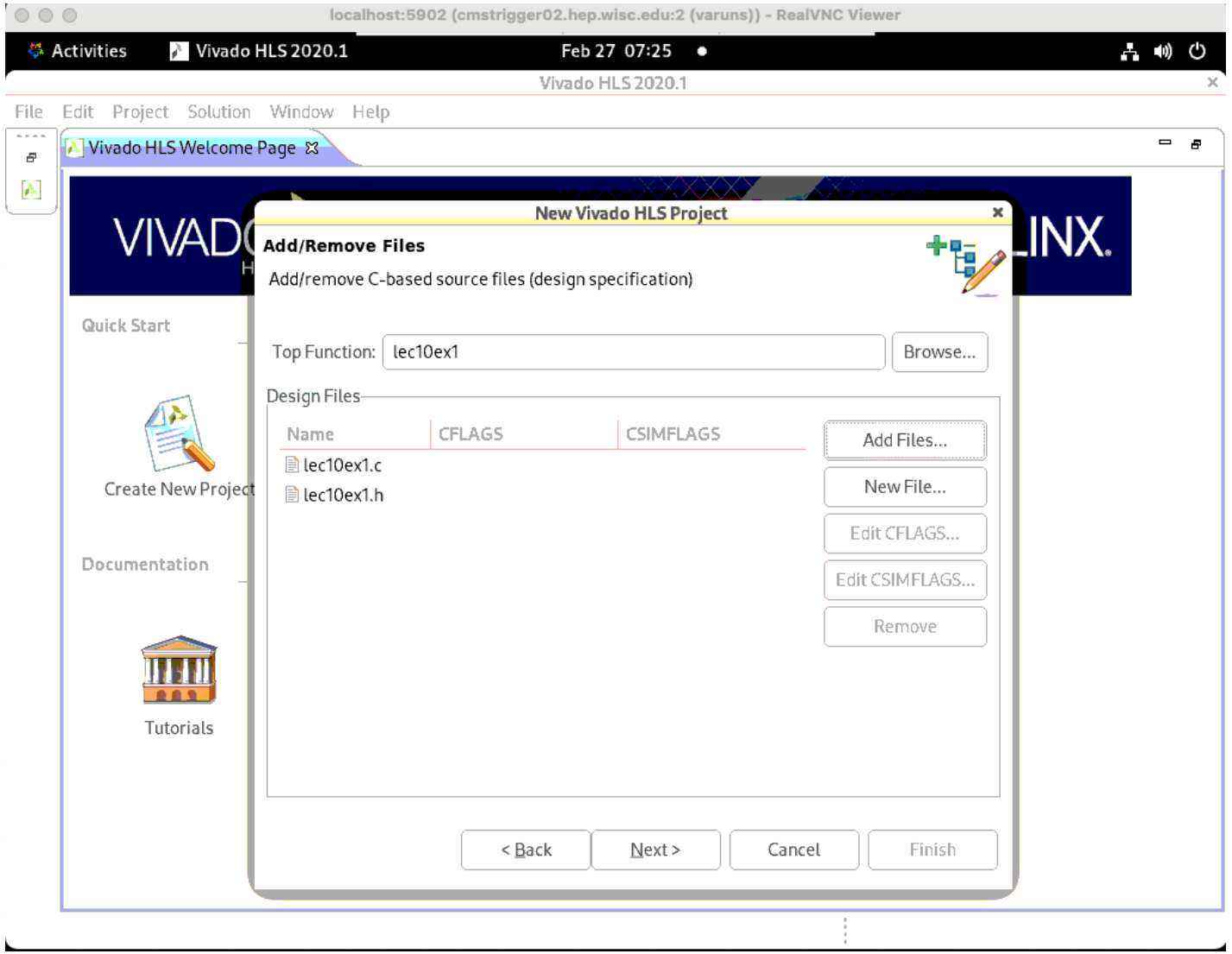
Creating Project

- Create New Project
- Enter the project name
- Click Browse to navigate to the location of the project directory
- Enter the location to be used for your project



Adding C-design

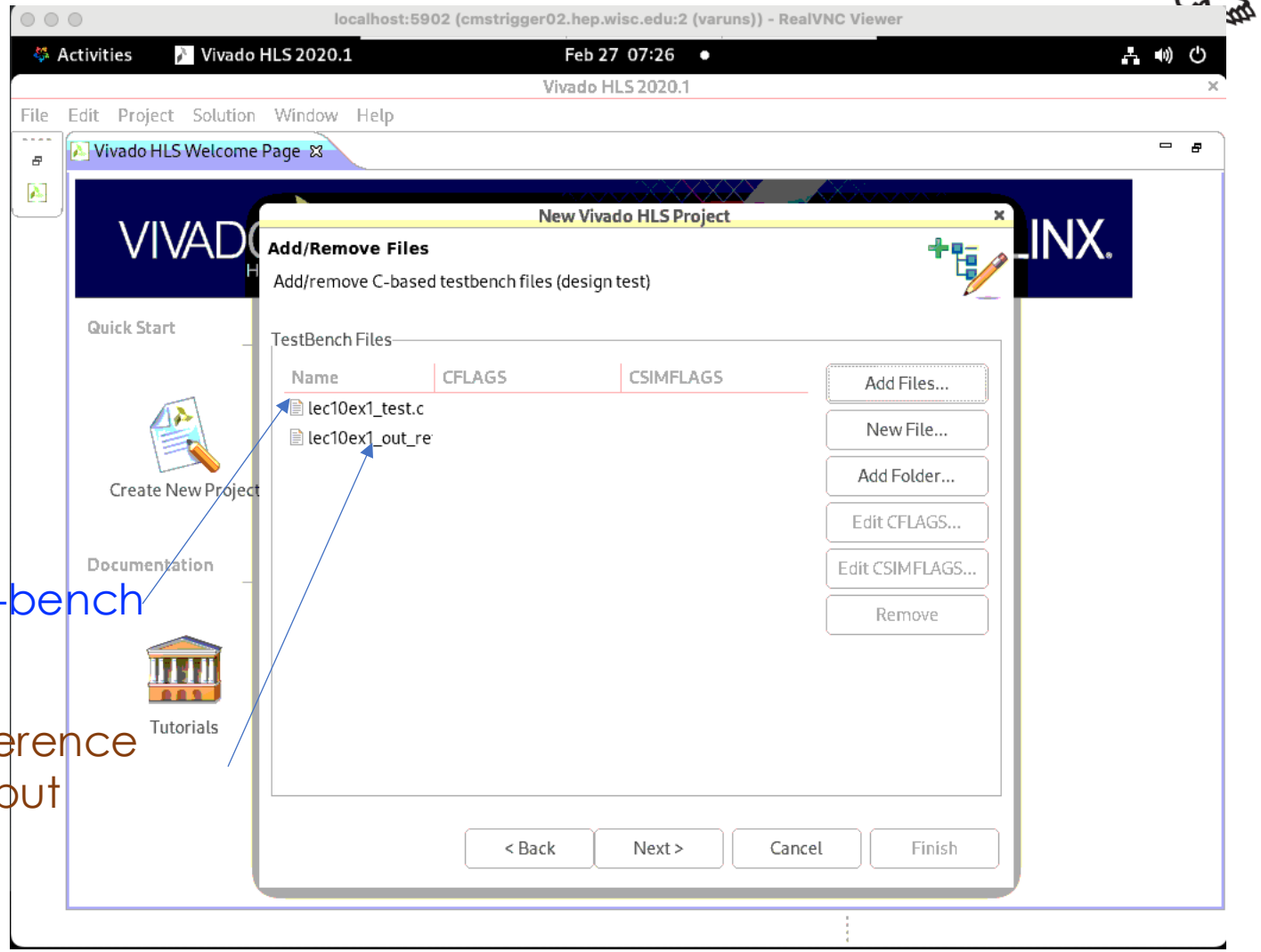
- Click Add Files
- Select all files that need to synthesized and click OK
- Specify the **top-level function** to be synthesised



Add test bench files

The test bench compares the output data from the **"top-level"** function with known good values

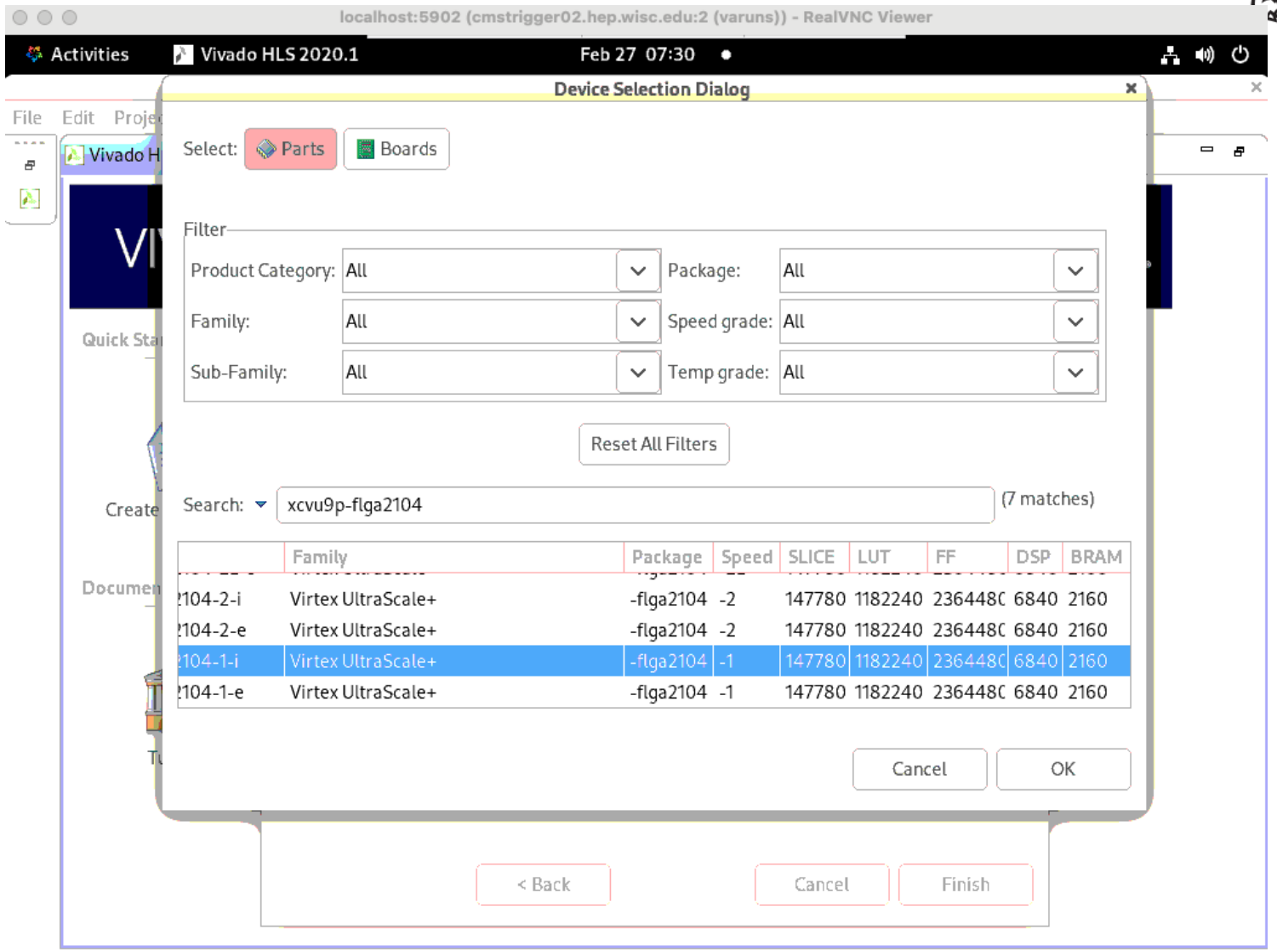
If you do not include all the files used by the test bench, **C** and **RTL simulation** might fail due to an inability to find the data files.



Select you target device

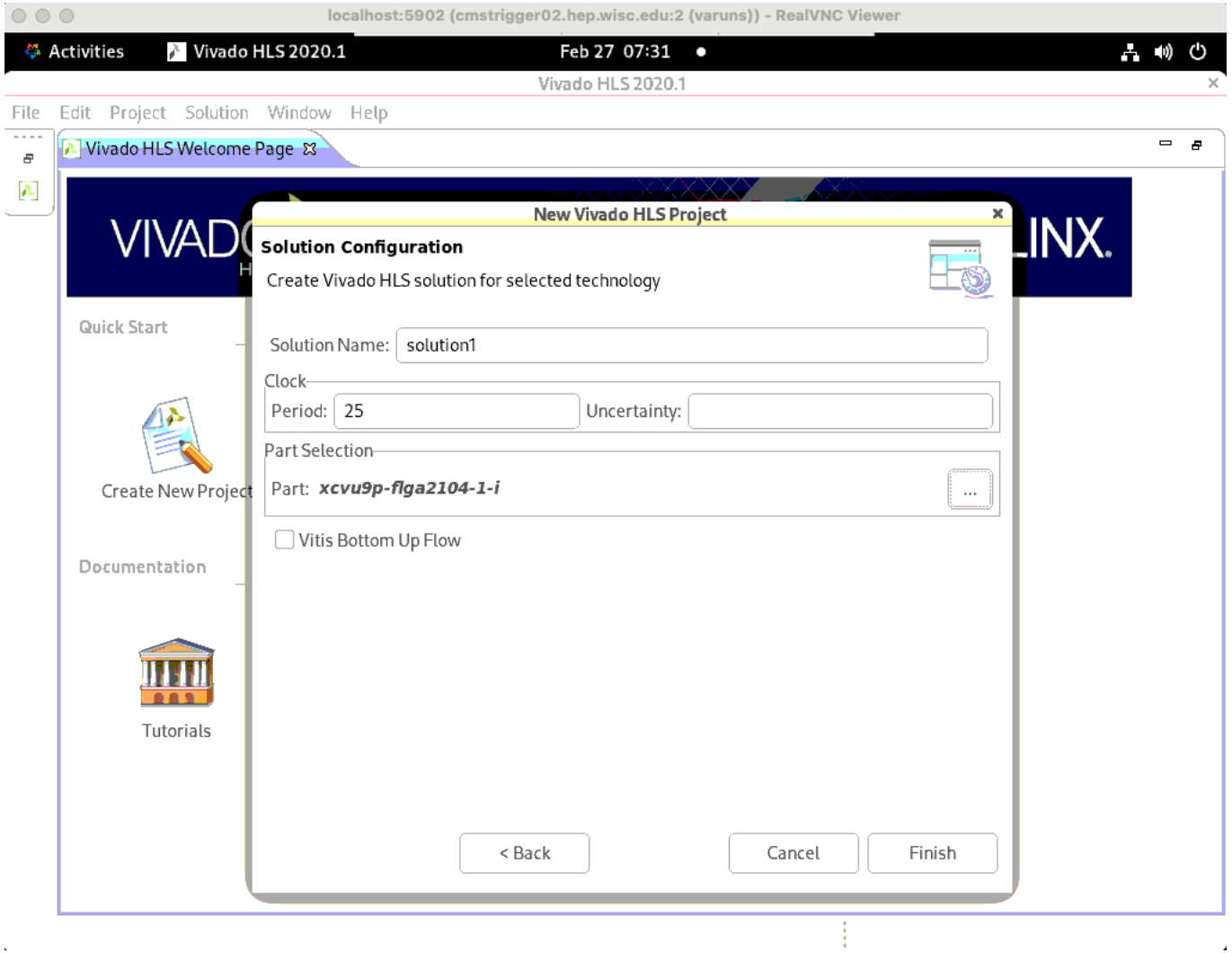
Check

- Family
- Package
- Speed grade,
- Resources available

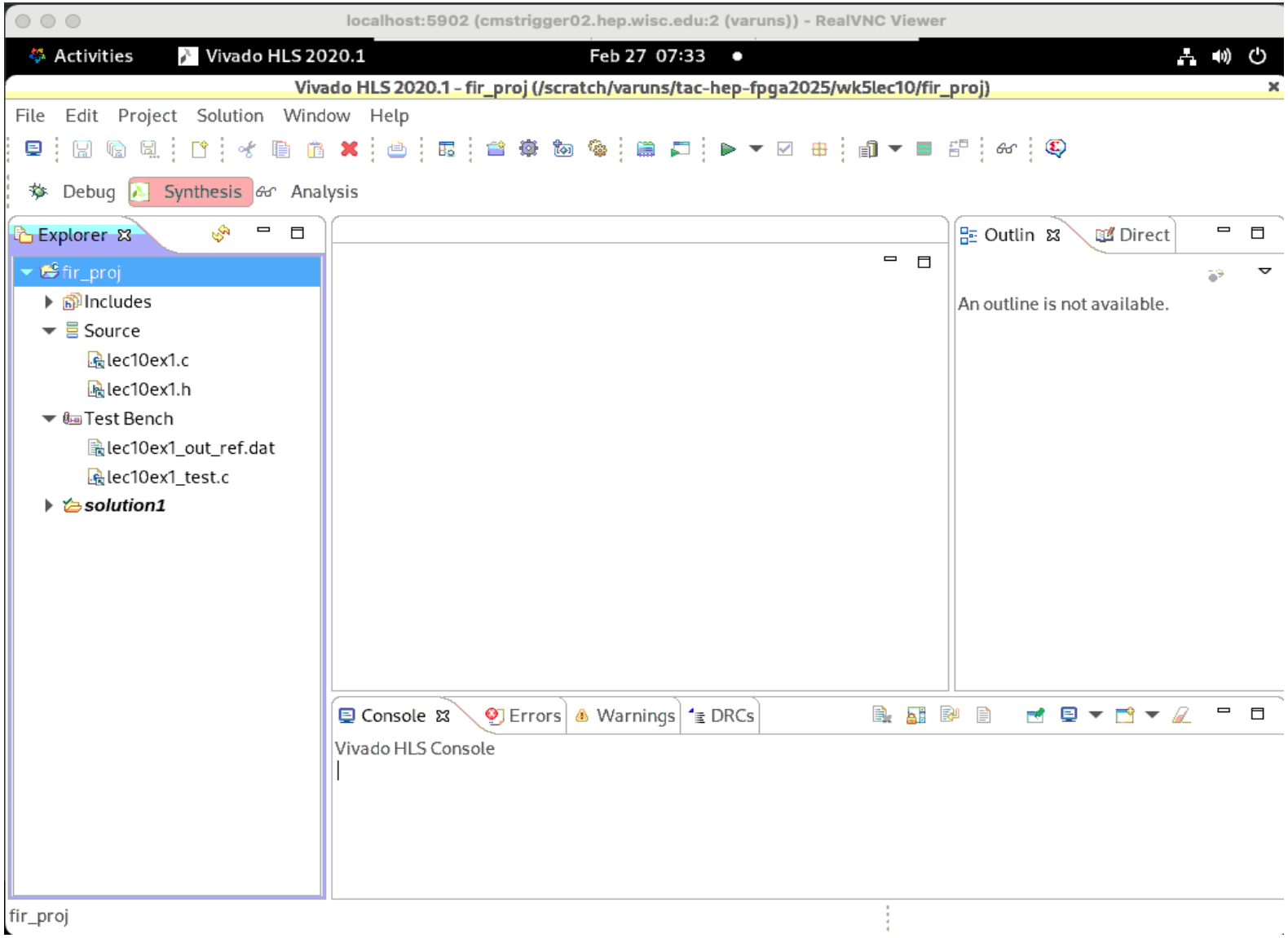


Target device

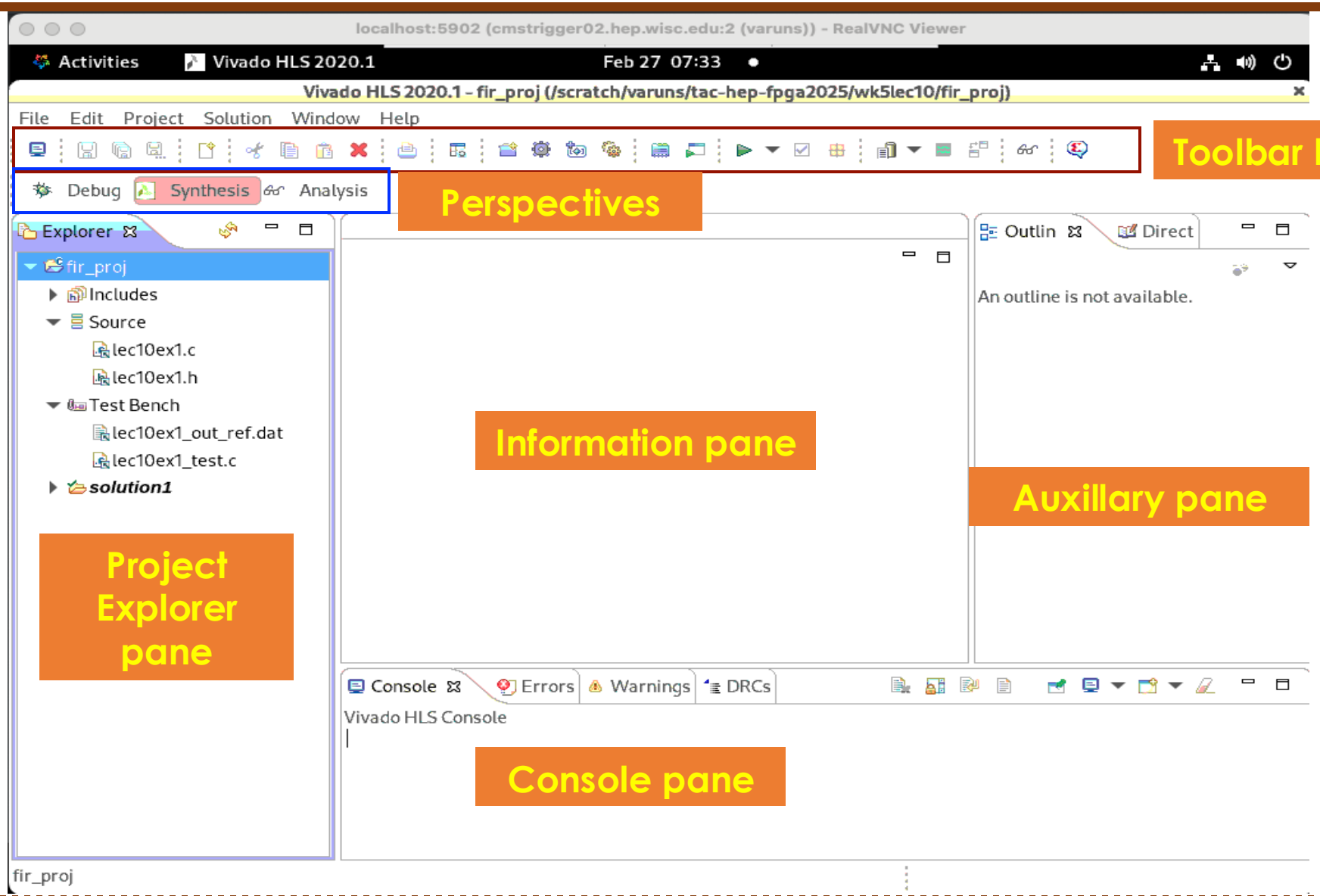
- **Solution Name**: of your choice
  - **solution1**
- **Clock Period**: in units of ns or a frequency value specified with the MHz suffix
  - **25ns**
- **Uncertainty**: If no value is given, default is 12.5%
- **Part**: Click to select the appropriate technology
  - **xcvu9p-flga2104-1-i**



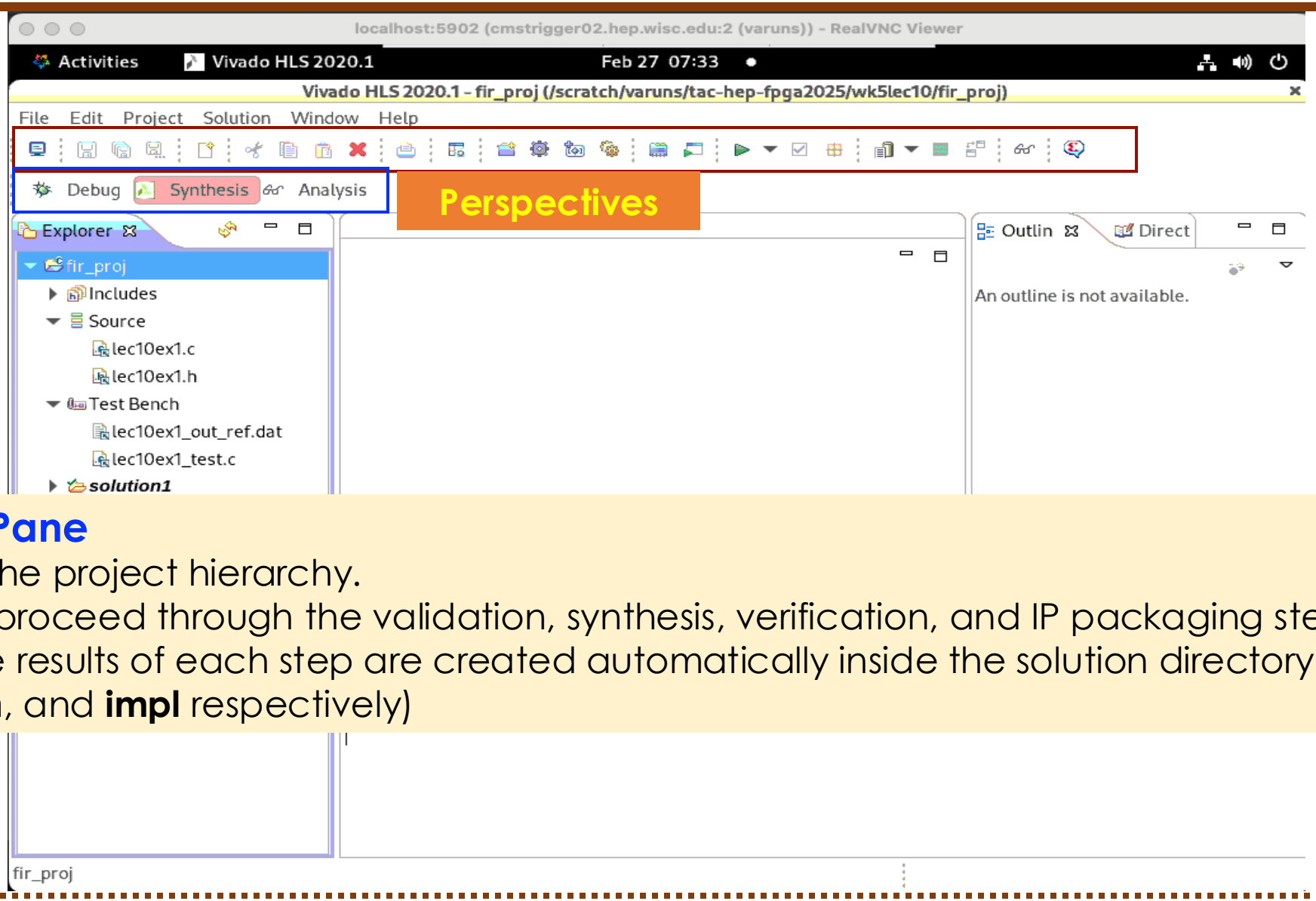
Vivado GUI


localhost:5902 (cmstrigger02.hep.wisc.edu:2 (varuns)) - RealVNC Viewer
Activities
Vivado HLS 2020.1
Feb 27 07:33
Vivado HLS 2020.1 - fir_proj (/scratch/varuns/tac-hep-fpga2025/wk5lec10/fir_proj)
File Edit Project Solution Window Help
Debug Synthesis Analysis
Explorer
fir_proj
Includes
Source
lec10ex1.c
lec10ex1.h
Test Bench
lec10ex1_out_ref.dat
lec10ex1_test.c
solution1
Outlin
Direct
An outline is not available.
Console
Errors
Warnings
DRCs
Vivado HLS Console
fir_proj

Understanding GUI



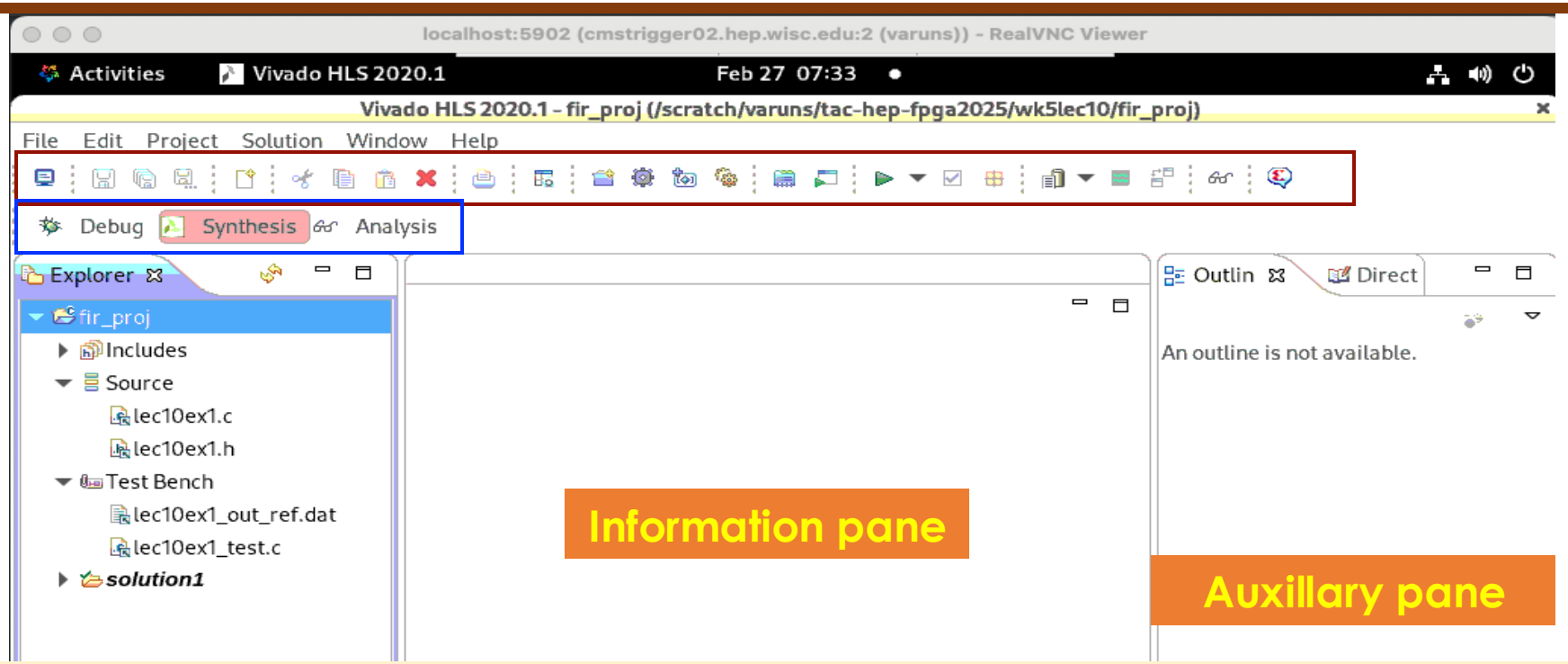
Understanding GUI



Explorer Pane

- Shows the project hierarchy.
- As you proceed through the validation, synthesis, verification, and IP packaging steps, sub-folders with the results of each step are created automatically inside the solution directory (named **csim**, **syn**, **sim**, and **impl** respectively)

Understanding GUI



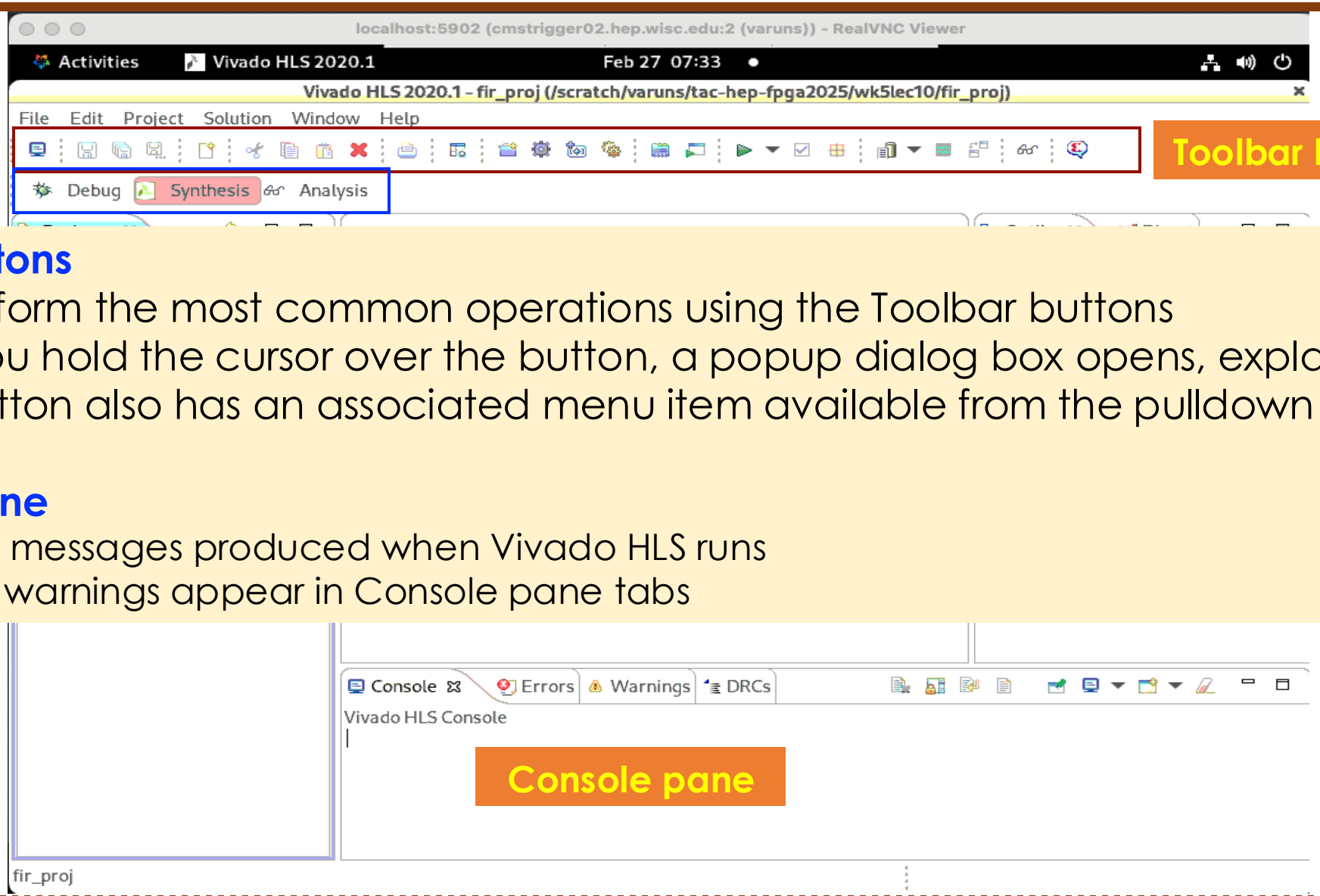
Information Pane

- Shows the contents of any files opened from the Explorer pane.
- When operations complete, the report file opens automatically in this pane

Auxiliary Pane

- Cross-links with the Information pane.
- The information shown in this pane dynamically adjusts, depending on the file open in the Information pane

Understanding GUI



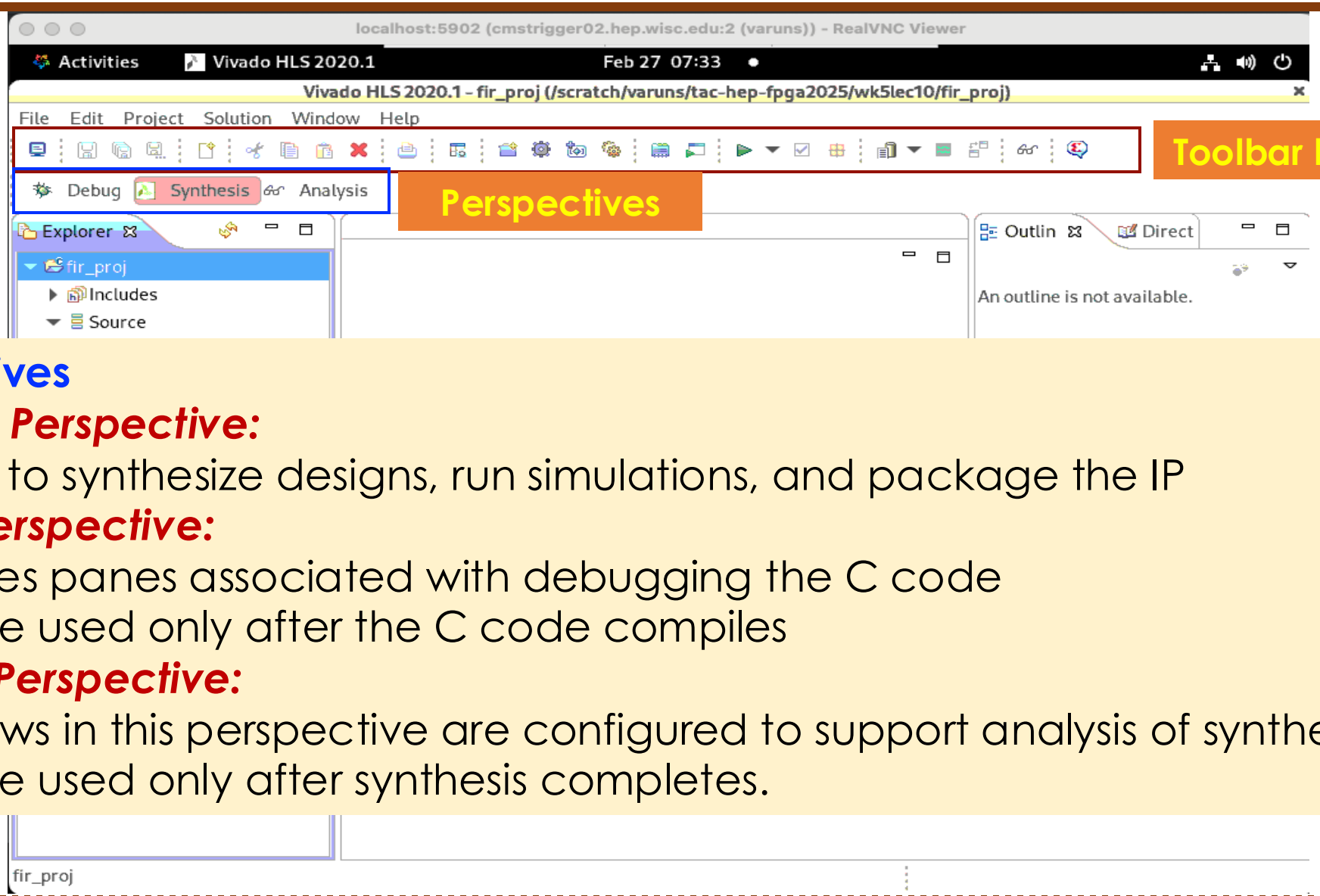
Toolbar Buttons

- Can perform the most common operations using the Toolbar buttons
- When you hold the cursor over the button, a popup dialog box opens, explaining the function
- Each button also has an associated menu item available from the pulldown menu

Console Pane

- Shows the messages produced when Vivado HLS runs
- Errors and warnings appear in Console pane tabs

Understanding GUI



Perspectives

Synthesis Perspective:

- Allows to synthesize designs, run simulations, and package the IP

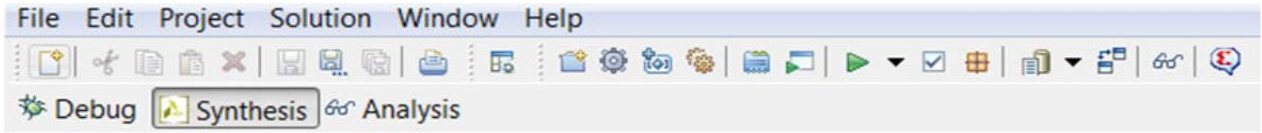
Debug Perspective:

- Includes panes associated with debugging the C code
- Can be used only after the C code compiles

Analysis Perspective:

- Windows in this perspective are configured to support analysis of synthesis results
- Can be used only after synthesis completes.

Toolbar buttons



- **Create New Project** opens the new project wizard
- **Project Settings** allows the current project settings to be modified
- **New Solution** opens the new solution dialog box
- **Solution Settings** allows the current solution settings to be modified

The next group of toolbar buttons control the tool operation:

- **Index C Source** refreshes the annotations in the C source
- **Run C Simulation** opens the C Simulation dialog box
- **C Synthesis** starts C source code in Vivado HLS
- **Run C/RTL Cosimulation** verifies the RTL output
- **Export RTL** packages the RTL into the desired IP output format

The final group of toolbar buttons are for design analysis:

- **Open Report** opens the C synthesis report or drops down to open other reports
- **Compare Reports** allows the reports from different solutions to be compared

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Example

https://github.com/varuns23/TAC-HEP-FPGA/tree/main/tutorial/wk5lec10

lec10ex1

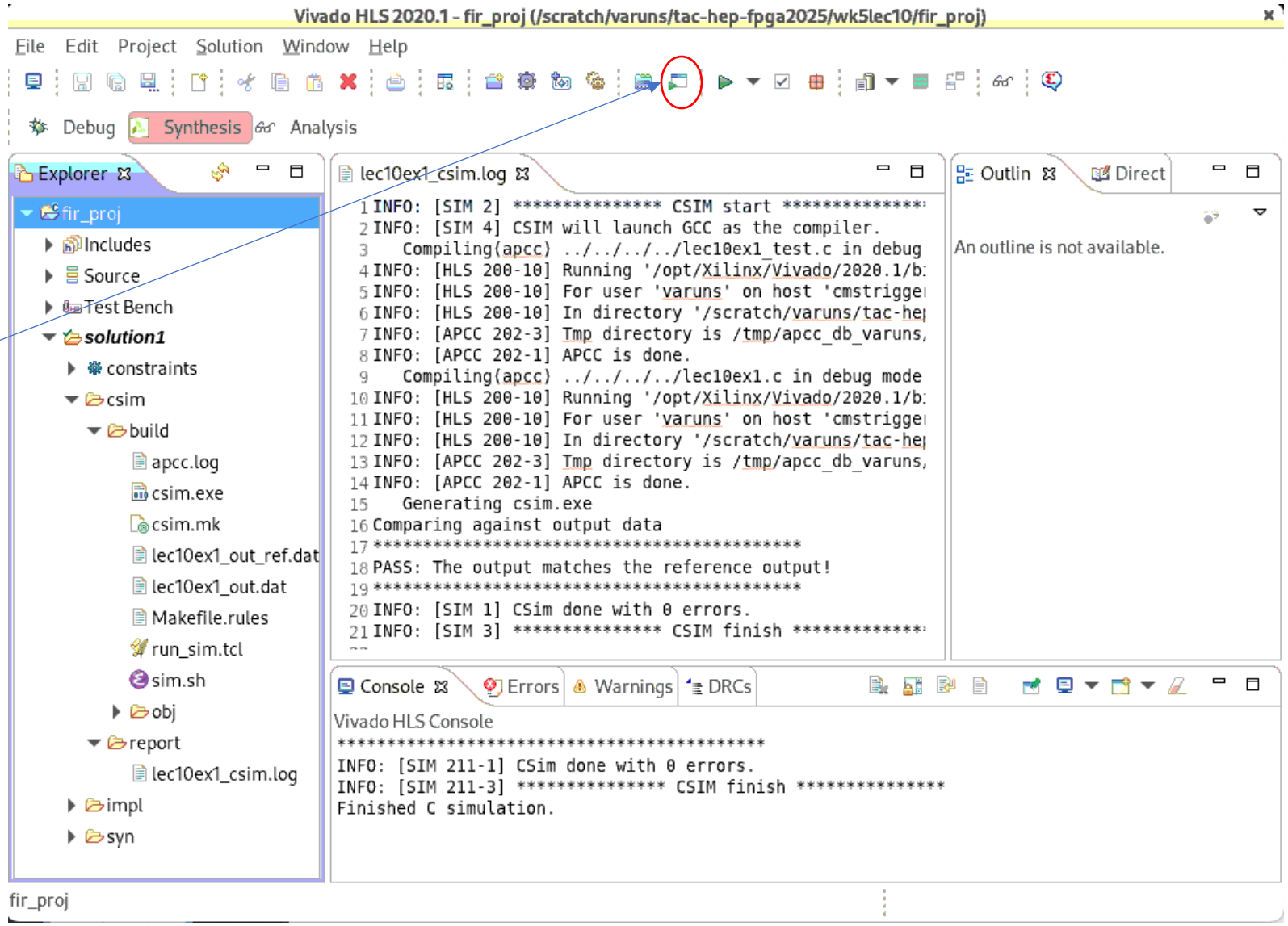
```c
#include "lec10ex1.h"

void lec10ex1 (int *y, int c[N],  int x) {

   static int arr[N];
   int sum;
   int data;
   int i;

   sum=0;
Loop:
   for (i = N - 1; i >= 0; i--)
   {
      if (i == 0)
      {
         arr[0] = x;
         data = x;
      }
      else
      {
         arr[i] = arr[i - 1];
         data = arr[i];
      }
      sum += data * c[i];
      ;
   }
   *y = sum;
}
```

```c
#ifndef LEC10EX1_H_
#define LEC10EX1_H_
#define N       11

void lec10ex1 (
   int *y,
   int c[N+1],
   int x
   );

#endif
```

```c
int main()
{
  const int samples = 600;
  FILE *oFile;

  int inp, output;
  int coef[N] = { 0, -10, -9, 23, 56, 63, 56, 23, -9, -10, 0};

  int i, rmp;
  inp = 0;
  rmp = 1;

  oFile = fopen("lec10ex1_out.dat", "w");
  for (i = 0; i <= samples; i++)
  {
    if (rmp == 1)
      inp = inp + 1;
    else
      inp = inp - 1;

    // Execute the function with latest input
    lec10ex1(&output, coef, inp);

    if ((rmp == 1) && (inp >= 75))
      rmp = 0;
    else if ((rmp == 0) && (inp <= -75))
      rmp = 1;

    // Save the results.
    fprintf(oFile, "%i %d %d\n", i, inp, output);
  }
  fclose(oFile);

  printf("Comparing against output data \n");
  if (system("diff -w lec10ex1_out.dat lec10ex1_out_ref.dat"))
  {

    fprintf(stdout, "*******************************************\n");
    fprintf(stdout, "FAIL: Output DOES NOT match the reference output\n");
    fprintf(stdout, "*******************************************\n");
    return 1;
```

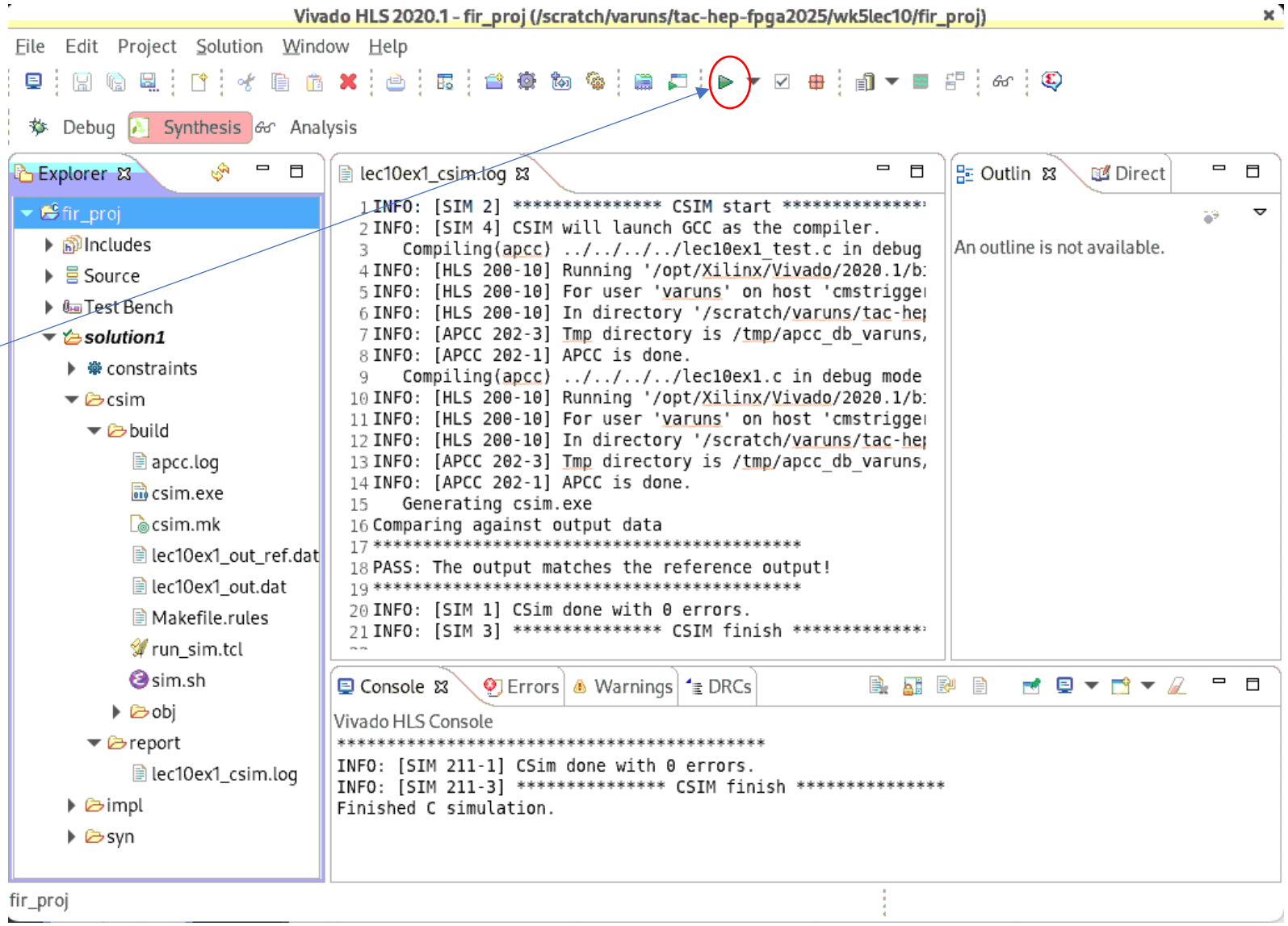
Step-2: C-Simulation

Run c-simulation



Step-3: C-Synthesis

Run C-Synthesis



Synthesis output printouts – 1/2

```
Starting C synthesis ...
/opt/Xilinx/Vivado/2020.1/bin/vivado_hls /scratch/varuns/tac-hep-fpga2025/wk5lec10/fir_proj/solution1/csynth.tcl
INFO: [HLS 200-10] Running '/opt/Xilinx/Vivado/2020.1/bin/unwrapped/lnx64.o/vivado_hls'
INFO: [HLS 200-10] For user 'varuns' on host 'cmstrigger02.hep.wisc.edu' (Linux_x86_64 version 5.14.0-427.22.1.el9_4
INFO: [HLS 200-10] In directory '/scratch/varuns/tac-hep-fpga2025/wk5lec10'
Sourcing Tcl script '/scratch/varuns/tac-hep-fpga2025/wk5lec10/fir_proj/solution1/csynth.tcl'
INFO: [HLS 200-10] Opening project '/scratch/varuns/tac-hep-fpga2025/wk5lec10/fir_proj'.
INFO: [HLS 200-10] Adding design file 'lec10ex1.c' to the project
INFO: [HLS 200-10] Adding design file 'lec10ex1.h' to the project
INFO: [HLS 200-10] Adding test bench file 'lec10ex1_out_ref.dat' to the project
INFO: [HLS 200-10] Adding test bench file 'lec10ex1_test.c' to the project
INFO: [HLS 200-10] Opening solution '/scratch/varuns/tac-hep-fpga2025/wk5lec10/fir_proj/solution1'.
INFO: [SYN 201-201] Setting up clock 'default' with a period of 25ns.
INFO: [HLS 200-10] Setting target device to 'xcvu9p-flga2104-1-i'
INFO: [SYN 201-201] Setting up clock 'default' with a period of 25ns.
INFO: [SCHED 204-61] Option 'relax_ii_for_timing' is enabled, will increase II to preserve clock frequency constrair
INFO: [HLS 200-10] Analyzing design file 'lec10ex1.c' ...
INFO: [HLS 200-111] Finished Linking Time (s): cpu = 00:00:15 ; elapsed = 00:00:14 . Memory (MB): peak = 1629.840 ;
INFO: [HLS 200-111] Finished Checking Pragmas Time (s): cpu = 00:00:15 ; elapsed = 00:00:14 . Memory (MB): peak = 16
INFO: [HLS 200-10] Starting code transformations ...
INFO: [HLS 200-111] Finished Standard Transforms Time (s): cpu = 00:00:16 ; elapsed = 00:00:16 . Memory (MB): peak =
INFO: [HLS 200-10] Checking synthesizability ...
INFO: [HLS 200-111] Finished Checking Synthesizability Time (s): cpu = 00:00:16 ; elapsed = 00:00:16 . Memory (MB):
INFO: [HLS 200-111] Finished Pre-synthesis Time (s): cpu = 00:00:16 ; elapsed = 00:00:16 . Memory (MB): peak = 1629.
INFO: [HLS 200-472] Inferring partial write operation for 'arr' (lec10ex1.c:16:10)
INFO: [HLS 200-472] Inferring partial write operation for 'arr' (lec10ex1.c:21:10)
INFO: [HLS 200-111] Finished Architecture Synthesis Time (s): cpu = 00:00:16 ; elapsed = 00:00:16 . Memory (MB): pea
INFO: [HLS 200-10] Starting hardware synthesis ...
INFO: [HLS 200-10] Synthesizing 'lec10ex1' ...
```

Synthesis output printouts – 2/2

Vivado HLS Console

```
INFO: [HLS 200-10] ----------------------------------------------------------------
INFO: [HLS 200-42] -- Implementing module 'lec10ex1'
INFO: [HLS 200-10] ----------------------------------------------------------------
INFO: [SCHED 204-11] Starting scheduling ...
INFO: [SCHED 204-11] Finished scheduling.
INFO: [HLS 200-111]  Elapsed time: 15.98 seconds; current allocated memory: 138.226 MB.
INFO: [BIND 205-100] Starting micro-architecture generation ...
INFO: [BIND 205-101] Performing variable lifetime analysis.
INFO: [BIND 205-101] Exploring resource sharing.
INFO: [BIND 205-101] Binding ...
INFO: [BIND 205-100] Finished micro-architecture generation.
INFO: [HLS 200-111]  Elapsed time: 0.04 seconds; current allocated memory: 138.392 MB.
INFO: [HLS 200-10] ----------------------------------------------------------------
INFO: [HLS 200-10] -- Generating RTL for module 'lec10ex1'
INFO: [HLS 200-10] ----------------------------------------------------------------
INFO: [RTGEN 206-500] Setting interface mode on port 'lec10ex1/y' to 'ap_vld'.
INFO: [RTGEN 206-500] Setting interface mode on port 'lec10ex1/c' to 'ap_memory'.
INFO: [RTGEN 206-500] Setting interface mode on port 'lec10ex1/x' to 'ap_none'.
INFO: [RTGEN 206-500] Setting interface mode on function 'lec10ex1' to 'ap_ctrl_hs'.
INFO: [RTGEN 206-100] Finished creating RTL model for 'lec10ex1'.
INFO: [HLS 200-111]  Elapsed time: 0.06 seconds; current allocated memory: 138.740 MB.
INFO: [HLS 200-790] **** Loop Constraint Status: All loop constraints were satisfied.
INFO: [HLS 200-789] **** Estimated Fmax: 173.25 MHz
INFO: [RTMG 210-278] Implementing memory 'lec10ex1_arr_ram (RAM)' using distributed RAMs with power-on initializati
INFO: [HLS 200-111] Finished generating all RTL models Time (s): cpu = 00:00:17 ; elapsed = 00:00:17 . Memory (MB):
INFO: [VHDL 208-304] Generating VHDL RTL for lec10ex1.
INFO: [VLOG 209-307] Generating Verilog RTL for lec10ex1.
INFO: [HLS 200-112] Total elapsed time: 17.1 seconds; peak allocated memory: 138.740 MB.
Finished C synthesis.
```

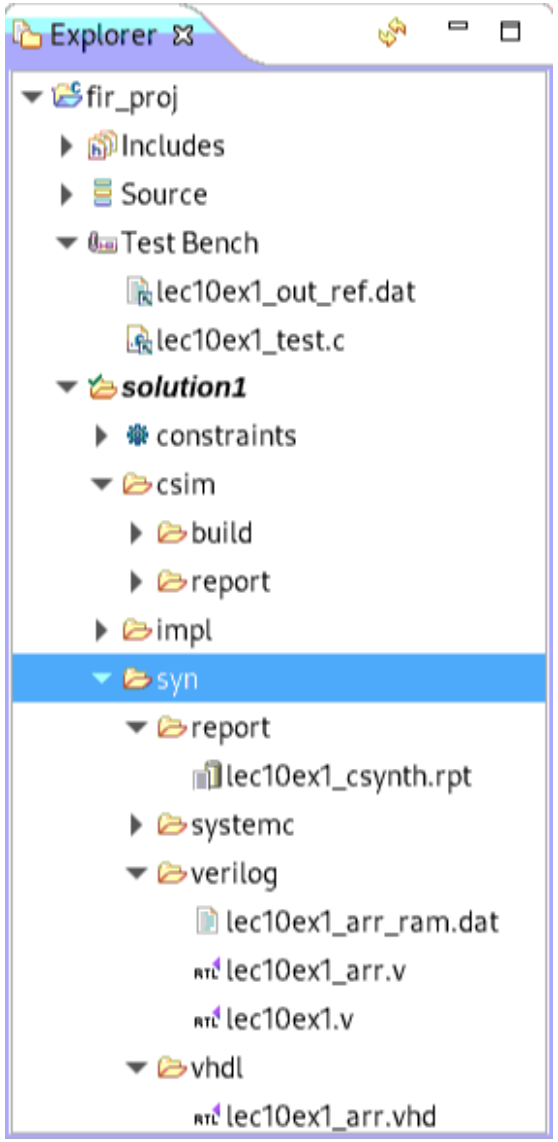
Step-3: Synthesis Report Review

The **syn** folder contains four sub-folder

A report folder and one folder for each of the RTL output formats.

The report folder contains a report file for the **top-level function** and one for every sub-function in the design

The **verilog**, **vhdl**, and **systemc** folders contain the output RTL files



Synthesis Report

Performance of the target device for desired algorithm

Synthesis(solution1)(lec10ex1_csynth.rpt) lec10ex1_test.c

Synthesis Report for 'lec10ex1'

General Information

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	25.00 ns	5.772 ns	3.12 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
34	34	0.850 us	0.850 us	34	34	none

Detail

Instance

N/A

Loop

	Latency (cycles)			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop	33	33	3	-	-	11	no

Synthesis Report: Resource Utilization

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	3	0	85	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	64	6	0
Multiplexer	-	-	-	105	-
Register	-	-	111	-	-
Total	0	3	175	196	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	0	~0	~0	~0	0
Utilization SLR (%)	0	~0	~0	~0	0

Synthesis Report: Interface Summary

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	lec10ex1	return value
ap_rst	in	1	ap_ctrl_hs	lec10ex1	return value
ap_start	in	1	ap_ctrl_hs	lec10ex1	return value
ap_done	out	1	ap_ctrl_hs	lec10ex1	return value
ap_idle	out	1	ap_ctrl_hs	lec10ex1	return value
ap_ready	out	1	ap_ctrl_hs	lec10ex1	return value
y	out	32	ap_vld	y	pointer
y_ap_vld	out	1	ap_vld	y	pointer
c_address0	out	4	ap_memory	c	array
c_ce0	out	1	ap_memory	c	array
c_q0	in	32	ap_memory	c	array
x	in	32	ap_none	x	scalar

Export the report(.html) using the Export Wizard

Open Analysis Perspective Analysis Perspective

Example for lecture 3

```
void foo(int in[3], char a, char b, char c, int out[3]) {
  int x,y;
  for(int i = 0; i < 3; i++) {
    x = in[i];
    y = a*x + b + c;
    out[i] = y;
  }
}
```

Assignment # 3

1. **Repeat the example on slide#20 with:**
   a. Target clock of 4ns
   b. Search for a new VU7 and VU13P device and see the estimates

2. **Create a project with example on slide#29**

Reminder: Assignments

- Assignment-1 (13-02-2025)
- Assignment-2 (18-02-2025)
- Assignment-3 (27-02-2025)

Uploaded to cernbox: https://cernbox.cern.ch/s/gmUqRDHTxDLqx4M

Send via email: **varun.sharma@cern.ch**

Submit in 2 weeks from date of assignment

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Extra slides

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Questions?

Acknowledgements:
- Some of these slides are from Isobel Ojalvo

Jargons

- **ICs - Integrated chip:** assembly of hundreds of millions of transistors on a minor chip
- **PCB:** Printed Circuit Board
- **LUT - Look Up Table aka 'logic'** - generic functions on small bitwidth inputs. Combine many to build the algorithm
- **FF - Flip Flops** - control the flow of data with the clock pulse. Used to build the pipeline and achieve high throughput
- **DSP - Digital Signal Processor** - performs multiplication and other arithmetic in the FPGA
- **BRAM - Block RAM** - hardened RAM resource. More efficient memories than using LUTs for more than a few elements
- **PCIe or PCI-E - Peripheral Component Interconnect Express**: is a serial expansion bus standard for connecting a computer to one or more peripheral devices
- **InfiniBand** is a computer networking communications standard used in high-performance computing that features very high throughput and very low latency
- **HLS** - High Level Synthesis - compiler for C, C++, SystemC into FPGA IP cores
- **HDL** - Hardware Description Language - low level language for describing circuits
- **RTL** - Register Transfer Level - the very low level description of the function and connection of logic gates
- **FIFO** – First In First Out memory
- **Latency** - time between starting processing and receiving the result
  - Measured in clock cycles or seconds
- **II - Initiation Interval** - time from accepting first input to accepting next input