Traineeships in Advanced Computing for High Energy Physics (TAC-HEP)

FPGA module training

Week-2: LHC, CMS Level-1 Trigger, & FPGAs in HEP

Lecture-3: February 4th 2025

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So Far…

- Motivation
- Comparison: FPGAs/ASICs/GPU/CPU
- Domain specific Accelerators

Today:

- LHC, CMS Experiment
- Level-1 Trigger
- FPGAs in HEP

What do we want?

Scientific discoveries

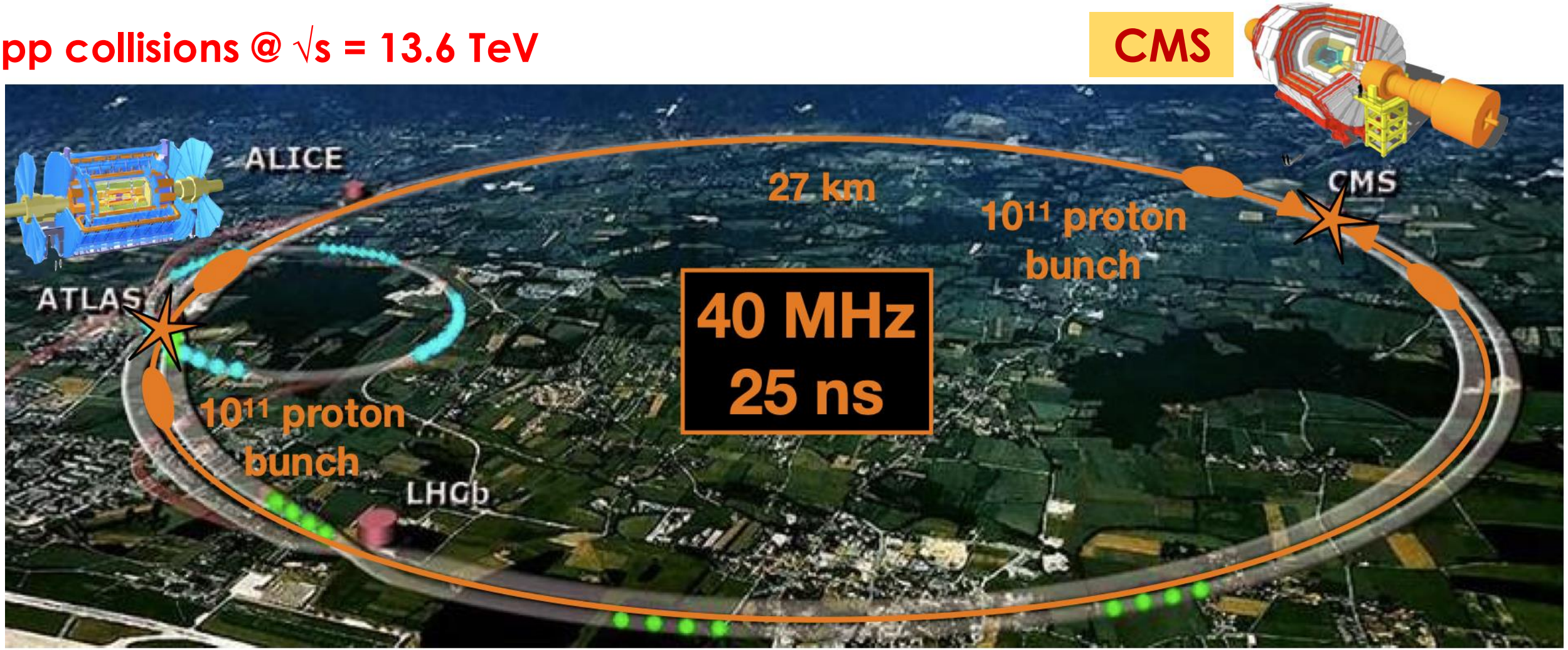
Journal Publications

TAC-HEP 2025

LHC, CMS Experiment

Large Hadron Collider

pp collisions @ √s = 13.6 TeV



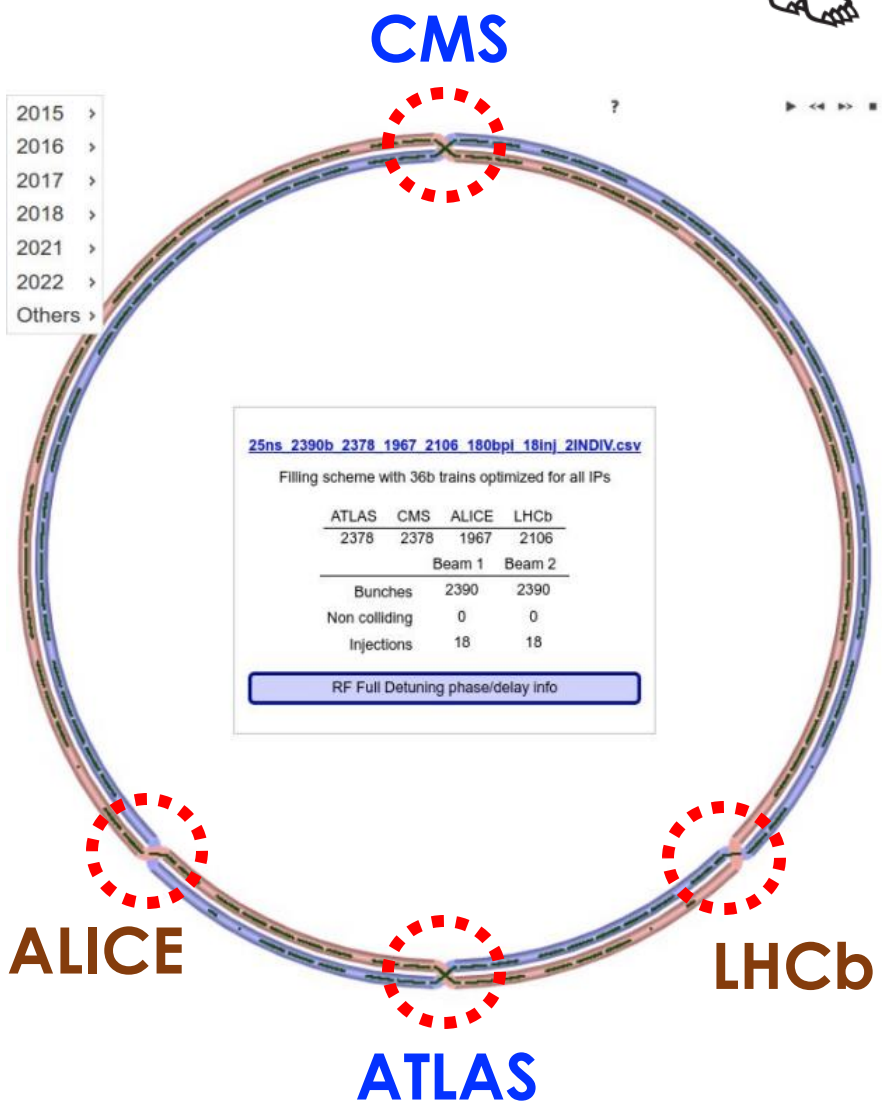
Large Hadron Collider

The LHC accelerates bunches of billions of protons (or ions) from 450 GeV injection energy from SPS to 6.8 TeV and collides them at **13.6 TeV** centre-of-mass energy

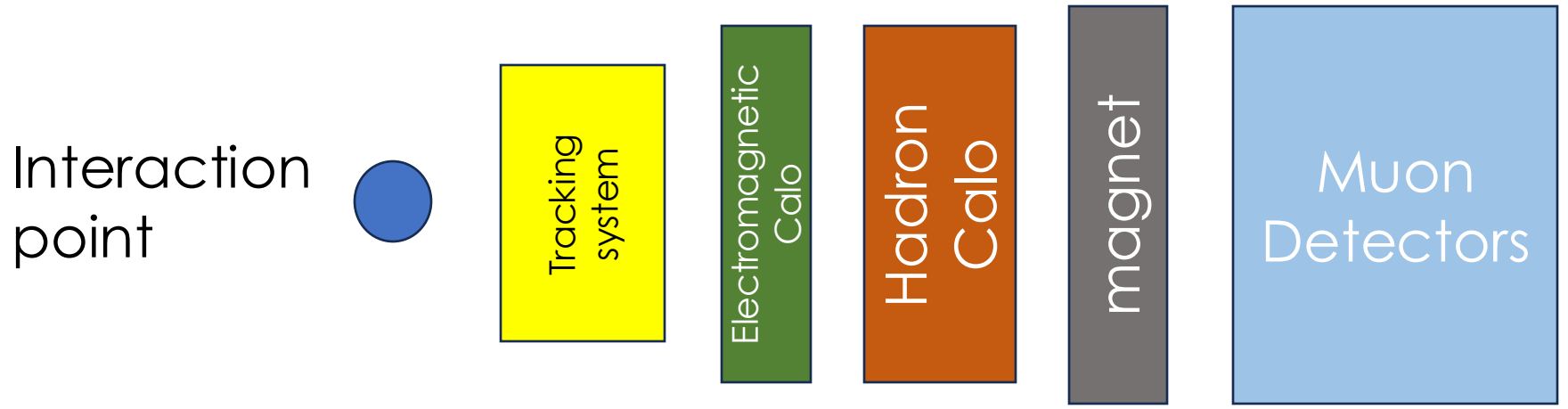
LHC circumference is 27km and the minimal distance between bunches is 25ns*c

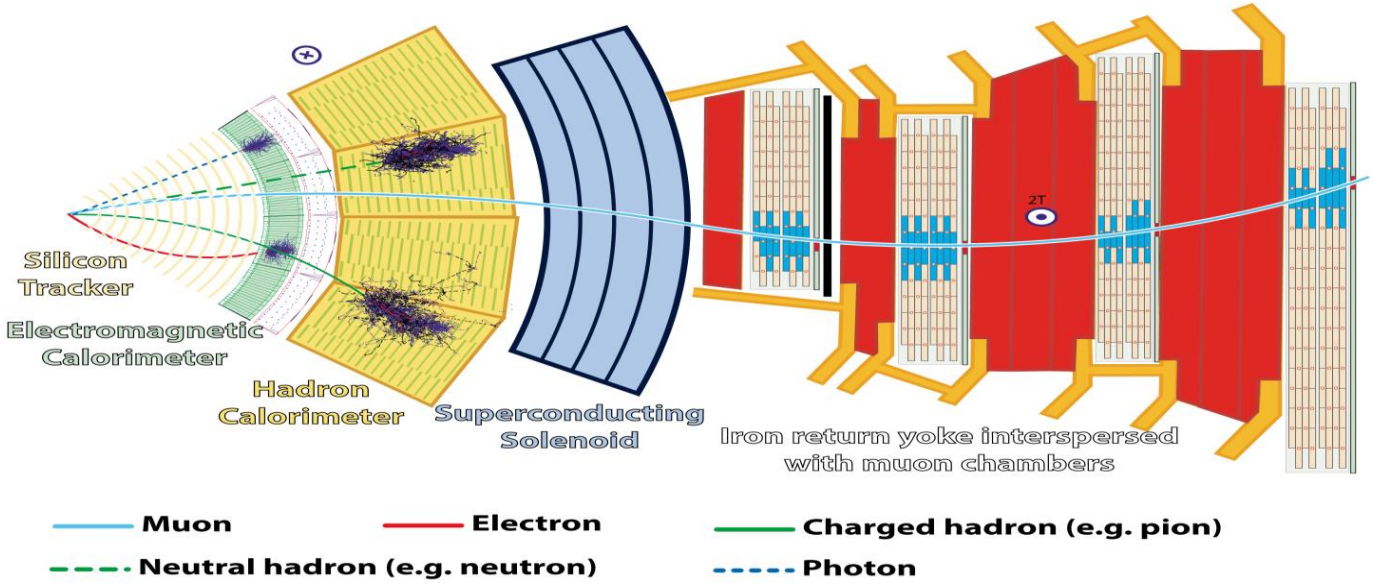
- Revolution frequency of LHC is 11.24 kHz
- Bunch crossing rate (ZeroBias rate) depends on number of bunches in the machine
- e.g. For 2380 colliding bunches (2023)
  - ZeroBias rate = 26.8 MHz

Filling scheme: 25ns_2352b_2340_2004_2133_108bpi_24inj

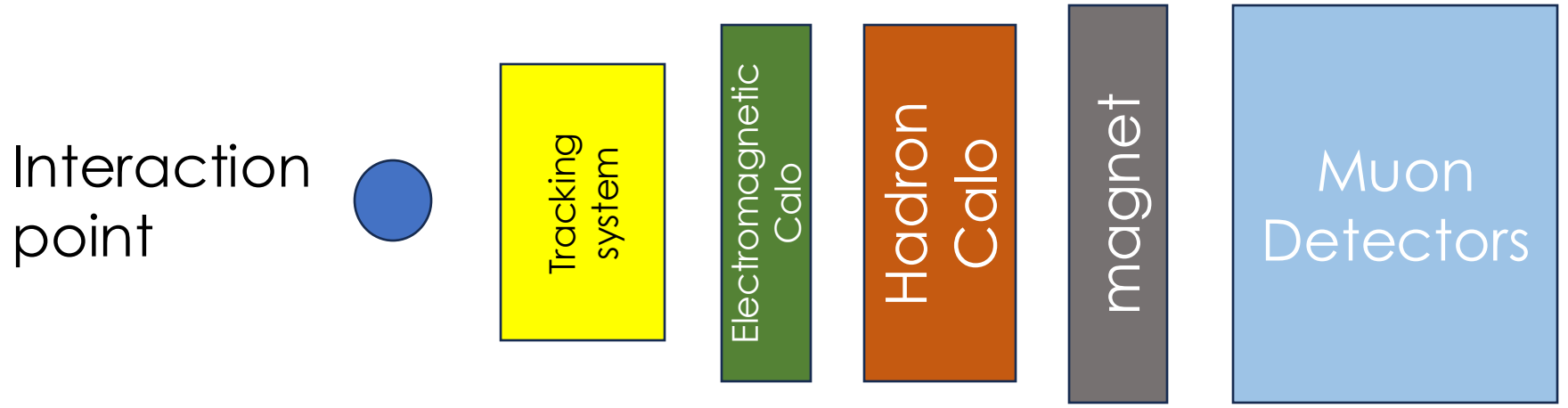


Particle Physics Detectors



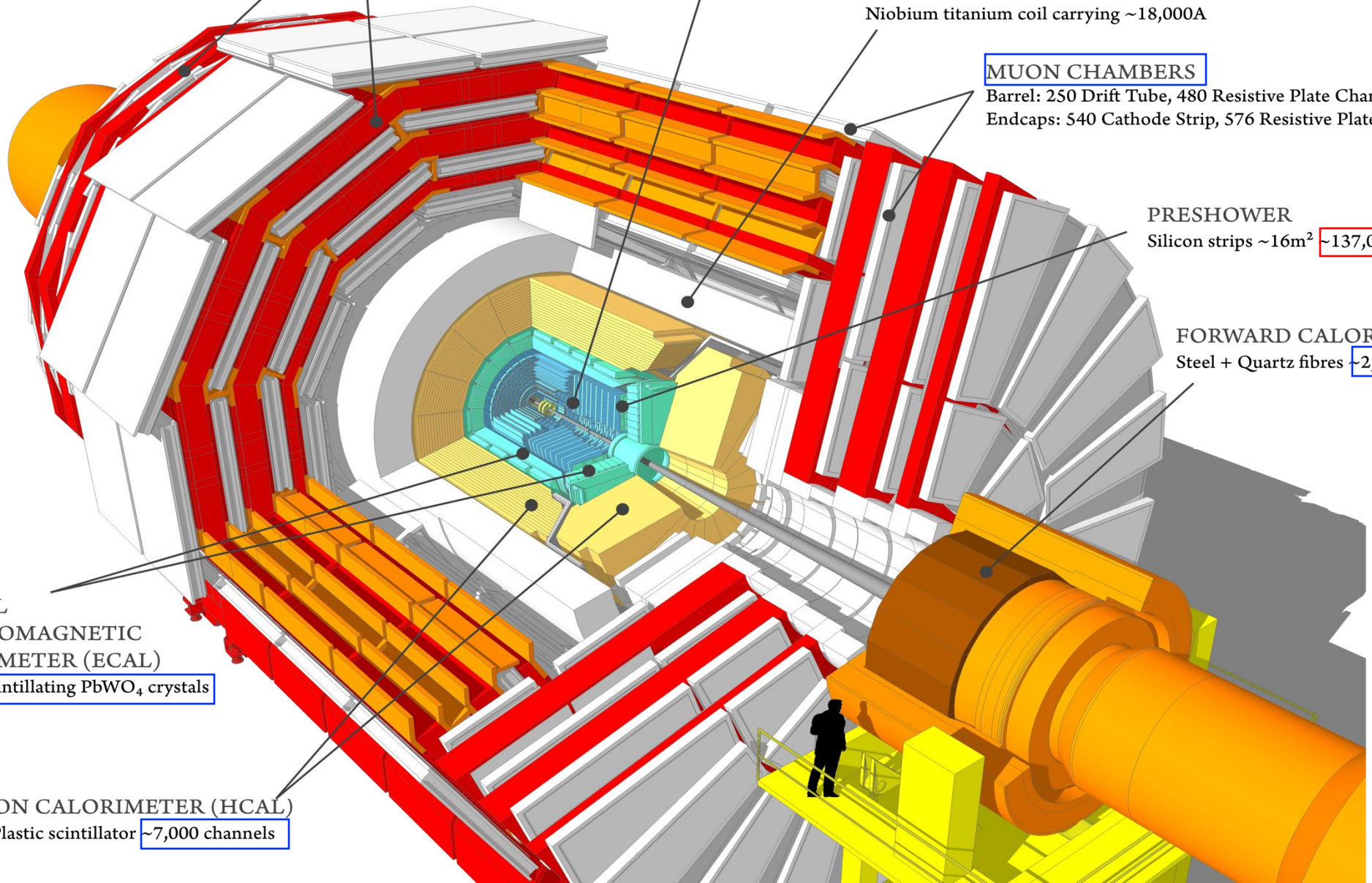


Example: CMS Detectors



CMS DETECTOR

Total weight : 14,000 tonnes
Overall diameter : 15.0 m
Overall length : 28.7 m
Magnetic field : 3.8 T



STEEL RETURN YOKE
12,500 tonnes

SILICON TRACKERS
Pixel (100x150 μm) ~1m² ~66M channels
Microstrips (80x180 μm) ~200m² ~9.6M channels

SUPERCONDUCTING SOLENOID
Niobium titanium coil carrying ~18,000A

MUON CHAMBERS
Barrel: 250 Drift Tube, 480 Resistive Plate Chambers
Endcaps: 540 Cathode Strip, 576 Resistive Plate Chambers

PRESHOWER
Silicon strips ~16m² ~137,000 channels

FORWARD CALORIMETER
Steel + Quartz fibres ~2,000 Channels

CRYSTAL ELECTROMAGNETIC CALORIMETER (ECAL)
~76,000 scintillating $PbWO_4$ crystals

HADRON CALORIMETER (HCAL)
Brass + Plastic scintillator ~7,000 channels

FPGAs/ASICs in CMS (ATLAS)

Front End Electronics (Detector Readout): Combination of ASICs+FPGA

- **ASICs:** Custom designed chips process signals from various detectors
  - **Calorimeters:** Measure energy deposits of particles
  - **Muon Chambers:** Detect muons
  - **Tracker:** Processes signal from silicon sensors
- **FPGAs:** Data handling and interfacing with DAQ

Data Acquisition (DAQ) and readout

- **FPGAs:** Handle high-speed data transmission, data formatting and interfacing with DAQ computers
- **ASICs:** Converting detector signals into digital data

Trigger System:

- **FPGAs:** Used extensively in the level-1 trigger to make ultra fast decisions (μs)

FPGAs/ASICs in other experiments

Neutrino Experiments:

- **ASICs:** Used in photodetectors (like PMTs, SiPMs) to convert light signals from neutrino interactions into digital data
- **FPGAs:** Used to filter & select neutrino events from background noise
  - Eg: **DUNE:** FPGAs in the DAQ system – Process vast amounts of data from the liquid argon detectors in real time

Dark matter experiments:

ASICs: Designed for ultra-low-noise signal processing in cryogenic enviroments

FPGAs: Real-time waveform analysis & triggering

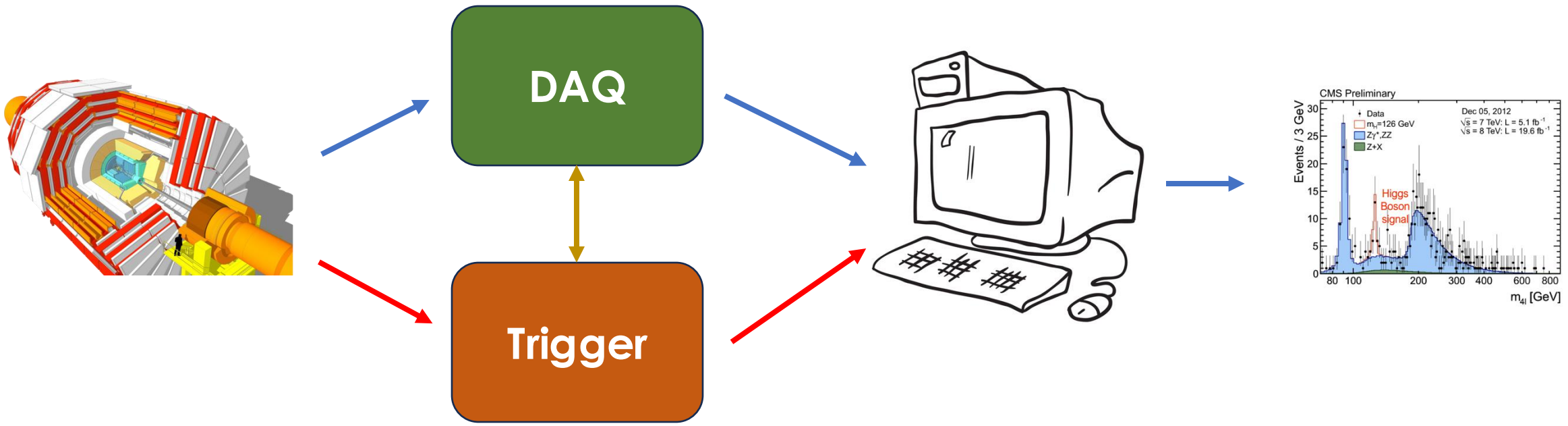
Eg: **LUX-ZEPLIN (LZ)**, FPGAs process PMT signal in real time to differentiate b/w potential DM interactions & bkg events

LHC Data flow…

- At an input rate of 40MHz
- Each raw event being 1-2MB

It is impossible to record data at 80 PB/s

Solution ⇒ Be Selective ⇒ Add a trigger



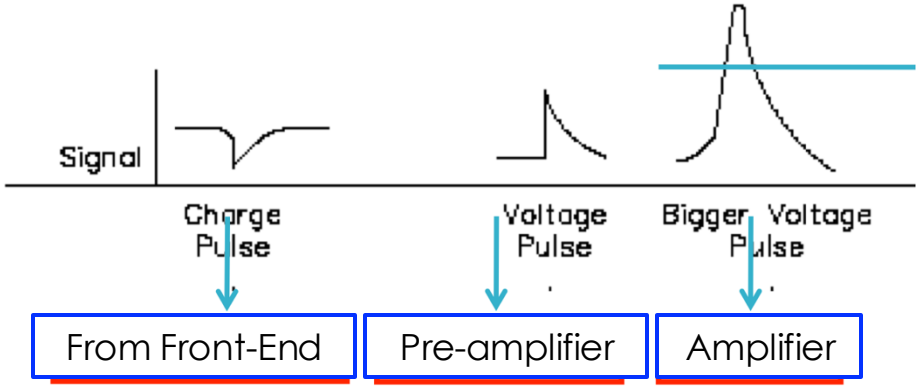
Trigger concept

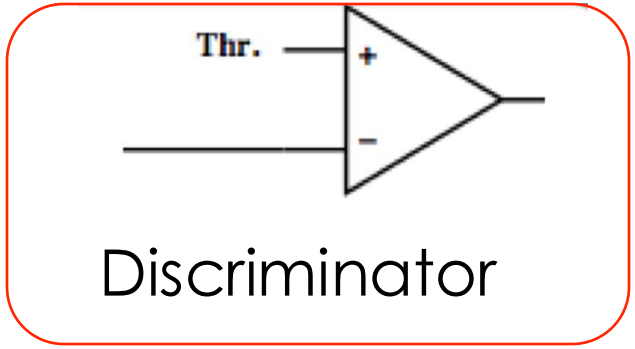
The role of the trigger is to make the **online selection** of particle collisions potentially containing interesting physics

- **What is 'Interesting'?:**
  - Define what is signal and what is background
- **What is the final affordable rate of the DAQ system?**
  - Define the maximum allowed rate
- **How fast the selection must be?**
  - Define the maximum allowed processing time

A Simple Trigger System

- **Data Input:** signals from front-end electronics



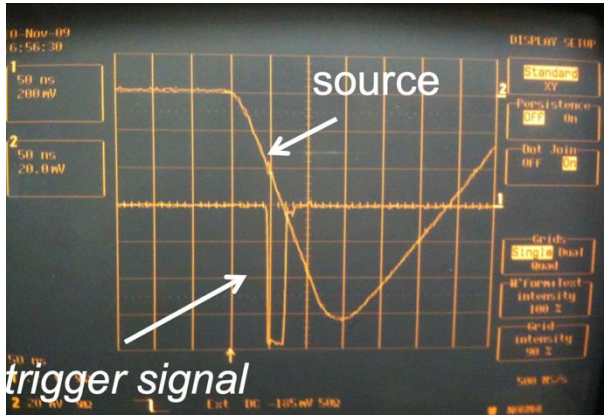


Accept

Reject

The simplest trigger: apply a threshold

- Look at the signal
- Put a threshold as low as possible

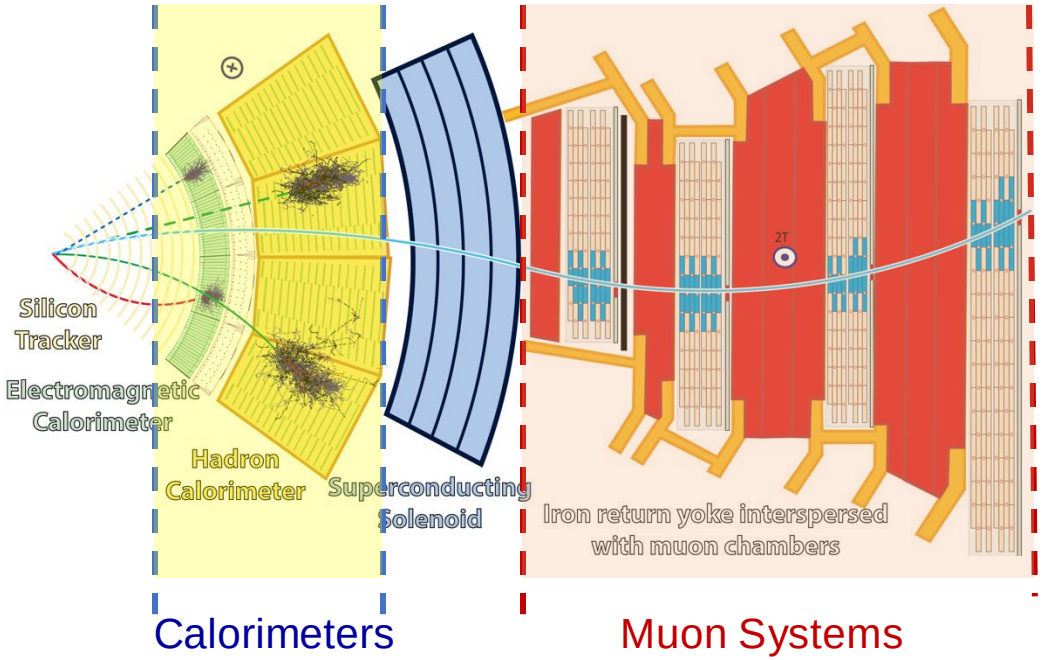


Input to CMS level-1 Trigger

Level-1 trigger receives data with coarse granularity from

- Calorimeters (ECAL, HCAL, HF)
- Muon systems (CSC, DT, RPC, GEM)

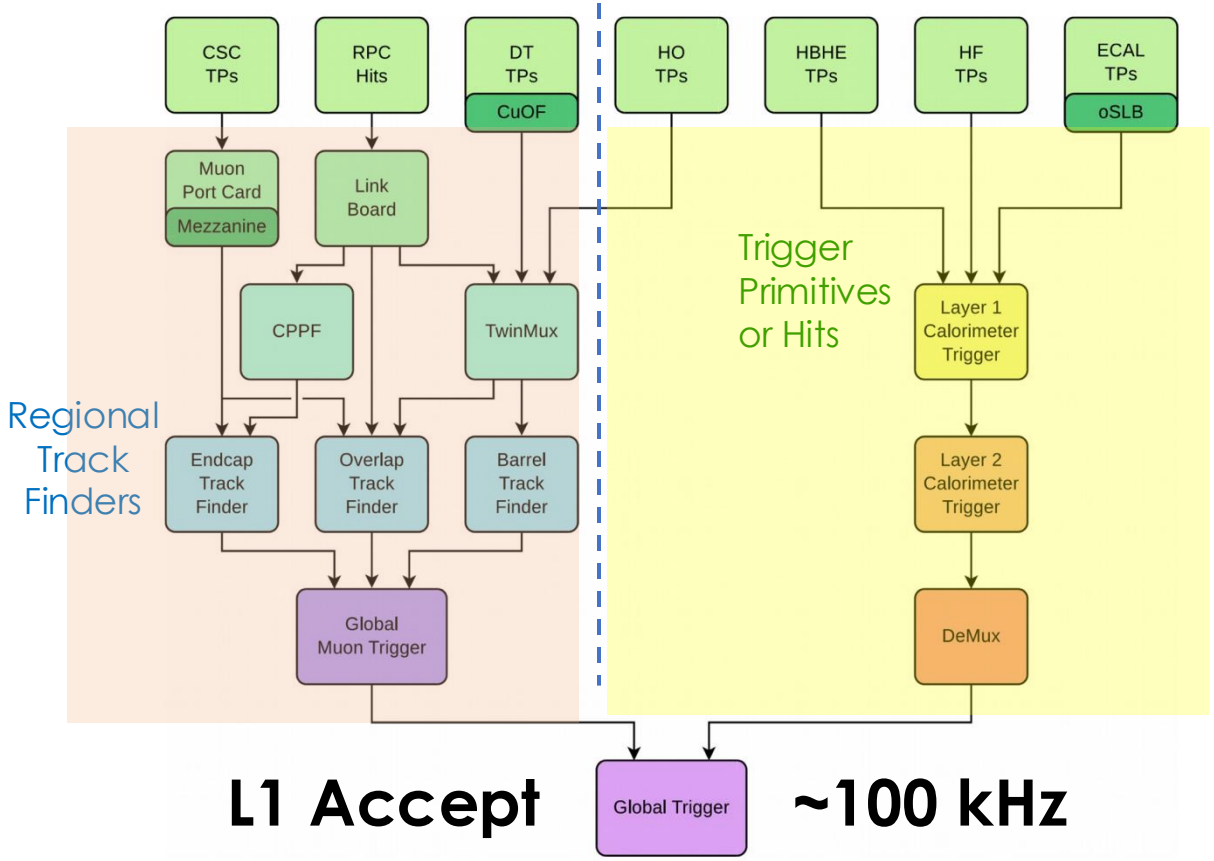
Collision data are buffered locally for < 4μs



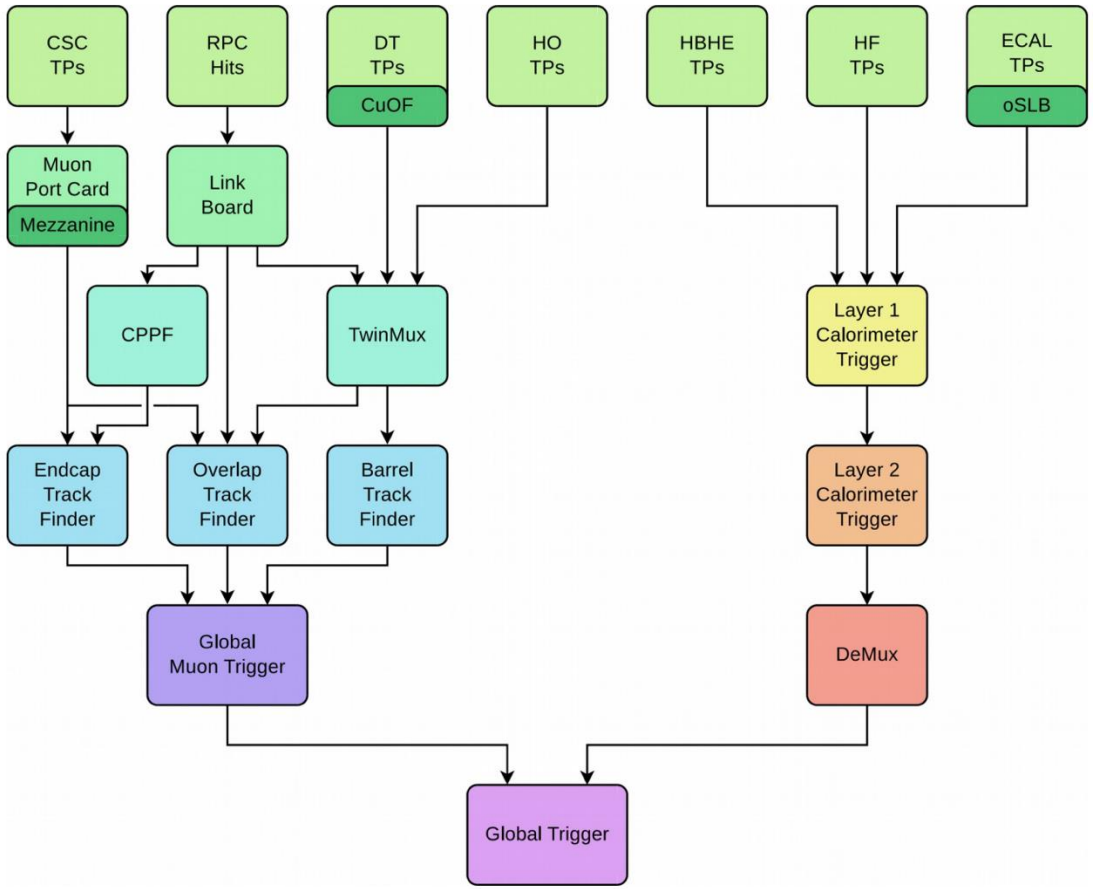
L1 Trigger is implemented in hardware

Uses field programmable gate arrays (FPGAs)

Operates synchronously to the LHC clock (40 MHz)



CMS Level-1 Trigger



To make decision in μs

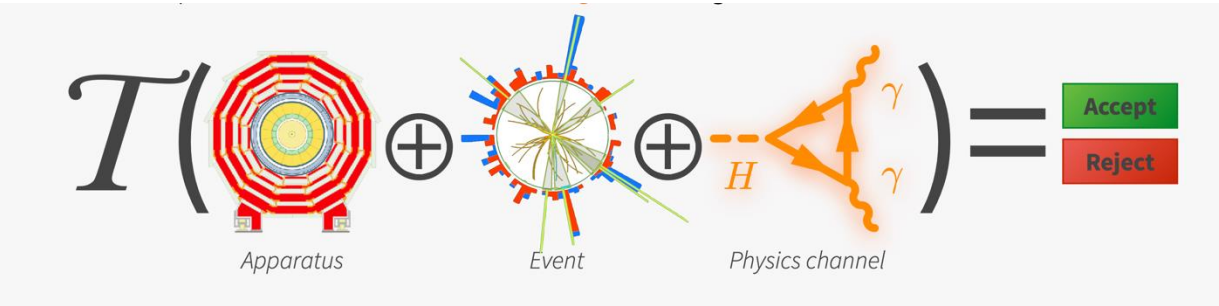
- We have parallel/Pipelined system
- Feed Forward Algorithms (no backward loops)
- Highly distributed
- Parallelism in FPGA
- Parallelism in Logic

CMS Trigger System

Two level triggering

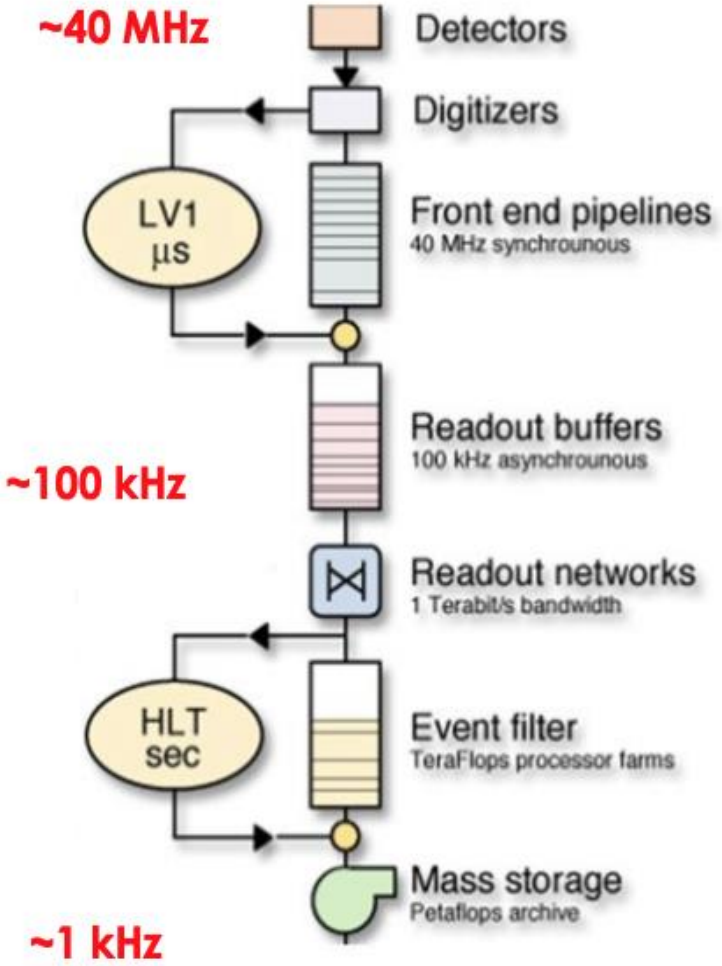
- *Level – 1 Trigger (L1T)*
  - Custom hardware using FPGAs
  - 40 MHz ➛ 100 kHz
- *High Level Trigger (HLT)*
  - Computing farm
  - 100 kHz ➛ 1kHz

Experiment	# of levels
ALICE	4
ATLAS	3
LHCb	3
CMS	2



Question: Why different levels?

CMS Trigger Architecture



Data path split here:
Coarse (L1), raw (DAQ)

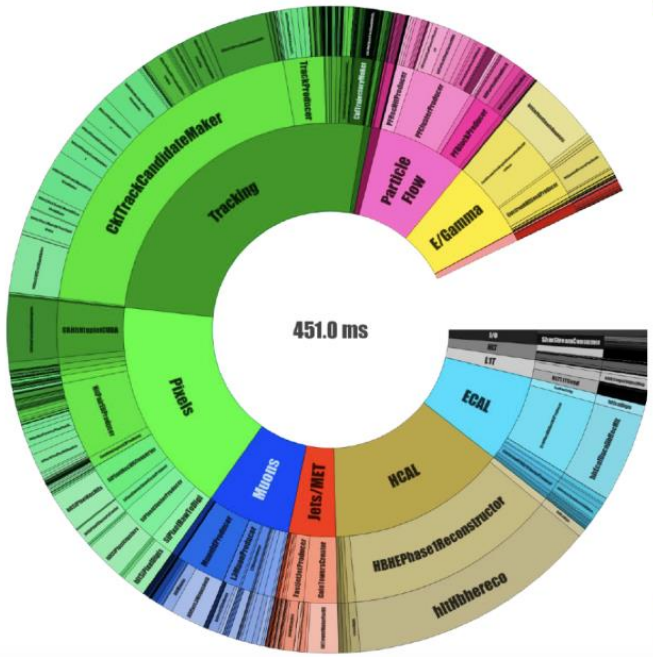
Data sitting in buffers,
waiting for decision from L1

L1 latency sets the depth of buffers (and $$)

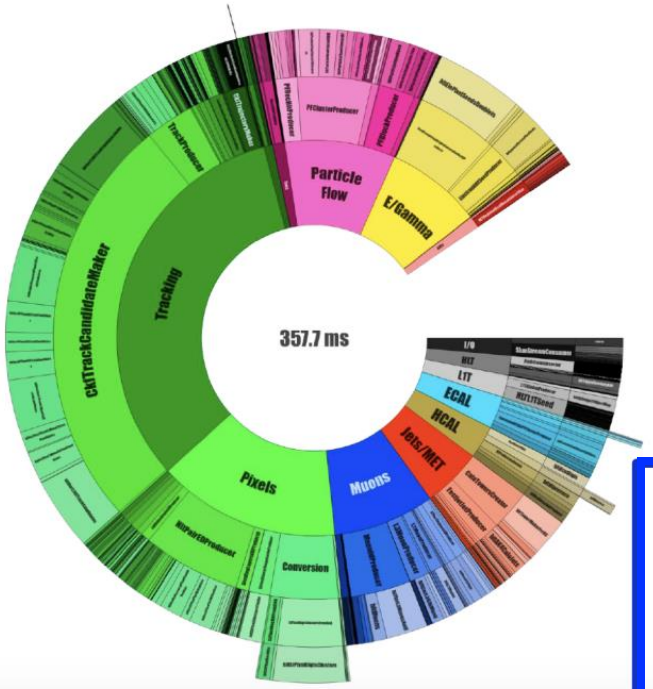
GPU Acceleration @ CMS HLT

21% processing time reduction

CPU



CPU + GPU



The pie-chart shows the distribution of CPU time in different instances of CMSSW modules (outermost ring), their corresponding C++ class (one level inner), grouped by physics object or detector (innermost ring). The empty slice indicates the time spent outside of the individual algorithms.

The time spent in the conversion of GPU-friendly *Structure of Arrays* data formats to legacy data formats is indicated by "Conversion" in the extra internal ring.

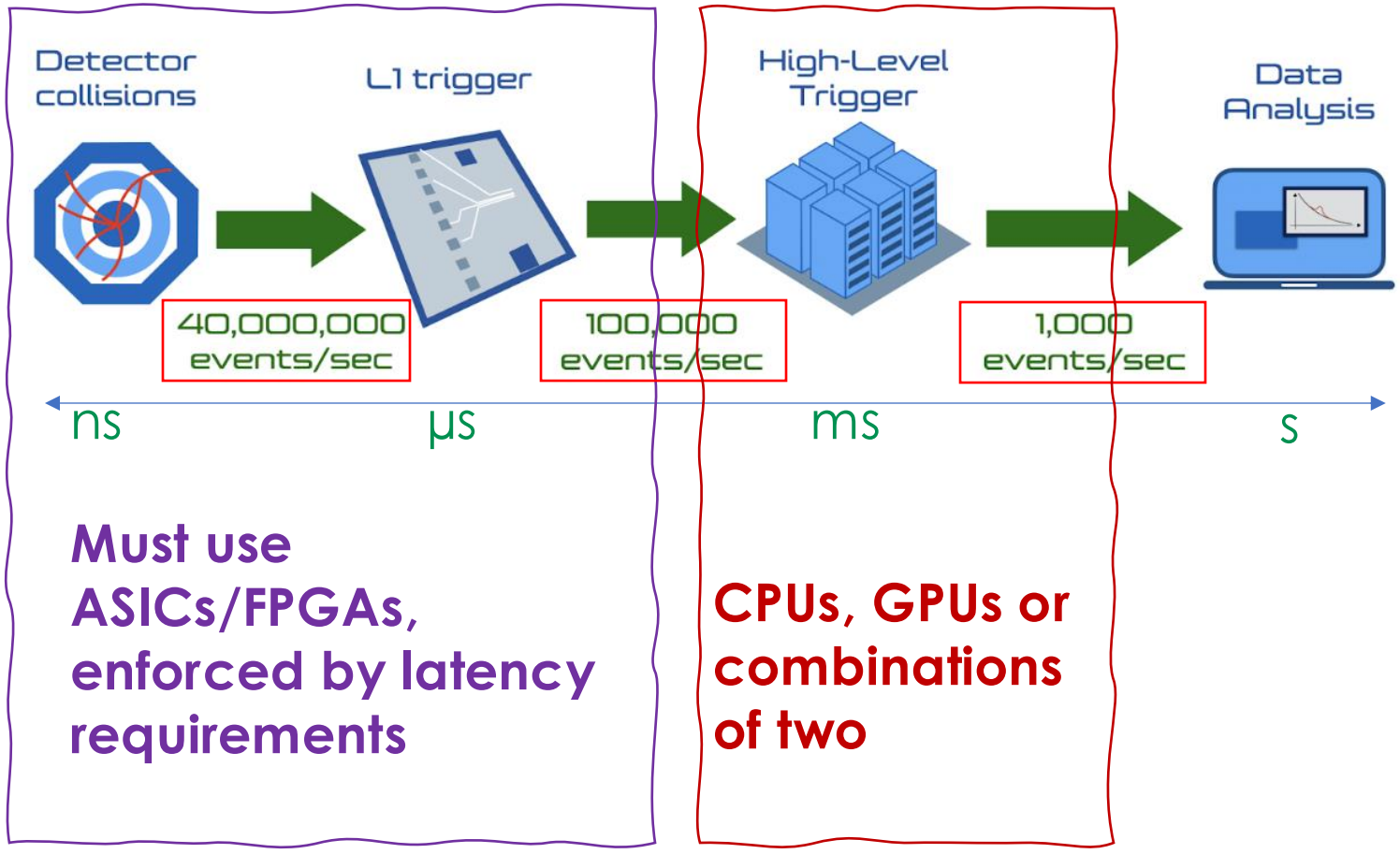
The timing is measured on pileup 50 events from Run2018D on a full HLT node (2x Intel Skylake Gold 6130) with HT enabled, running 16 jobs in parallel, with 4 threads each - equipped with an NVIDIA T4 GPU.

Using the GPU to accelerate:

- pixel local reconstruction, track and vertex reconstruction
- HCAL local reco (MAHI)
- ECAL unpacking and local reconstruction (multifit)

reduces the CPU usage by 21%, increasing the throughput by 26%.

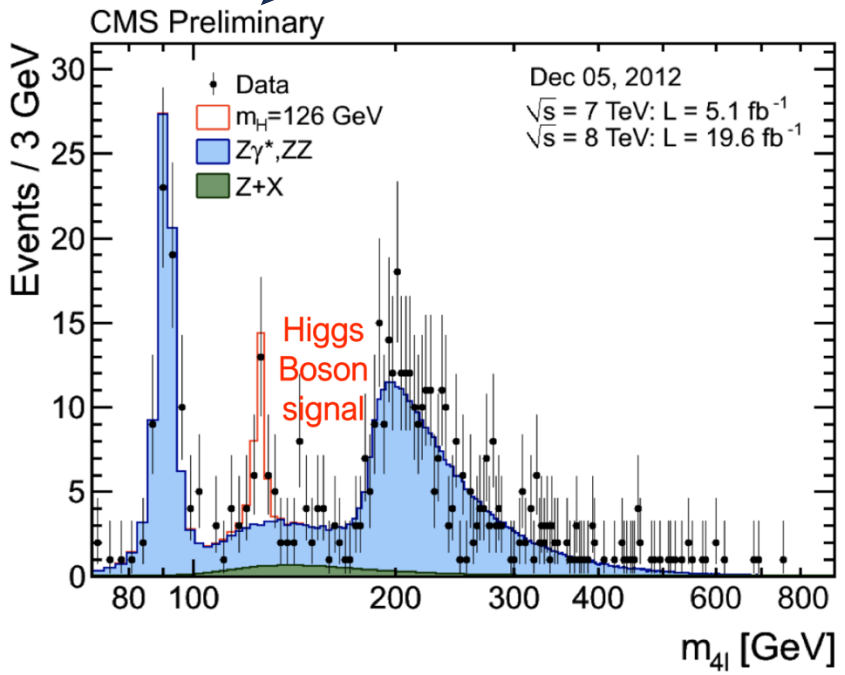
All set to do physics analyses

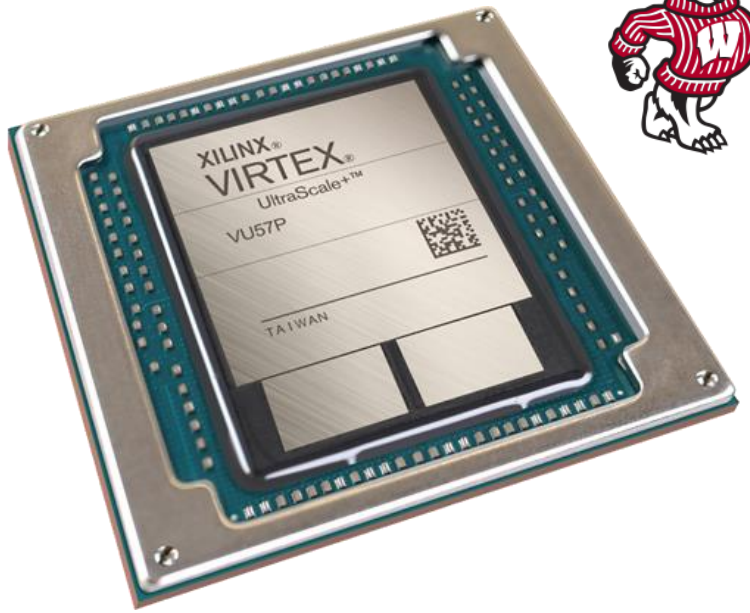


Must use ASICs/FPGAs, enforced by latency requirements

CPUs, GPUs or combinations of two

Months/Years





Lets discuss about FPGAs

FPGA: Field **P**rogrammable **G**ate **A**rray

Xilinx Field Programmable Gate Array

First FPGA invented by Xilinx Inc. in 1985

Gates [edit]

- 1987: 9,000 gates, Xilinx[6]
- 1992: 600,000, Naval Surface Warfare Department[3]
- Early 2000s: millions[8]
- 2013: 50 million, Xilinx[12]

Market size [edit]

- 1985: First commercial FPGA : Xilinx XC2064[5][6]
- 1987: $14 million[6]
- c. 1993: >$385 million[6][*failed verification*]
- 2005: $1.9 billion[13]
- 2010 estimates: $2.75 billion[13]
- 2013: $5.4 billion[14]
- 2020 estimate: $9.8 billion[14]
- 2030 estimate: $23.34 billion[15]

Design starts [edit]

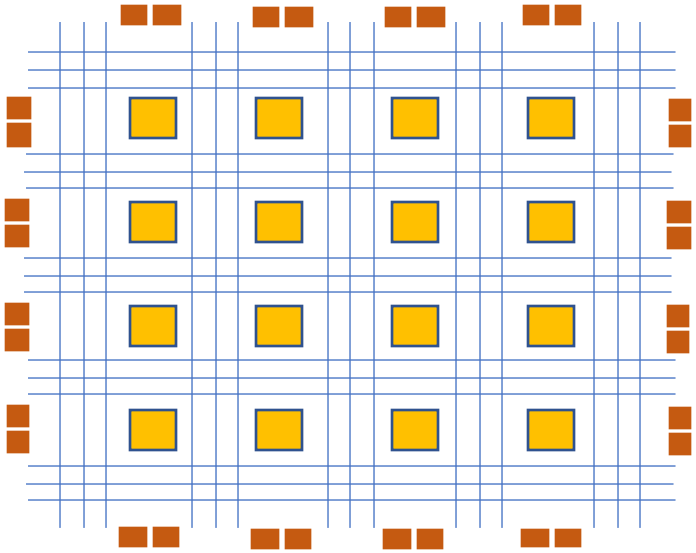
A *design start* is a new custom design for implementation on an FPGA.

- 2005: 80,000[16]
- 2008: 90,000[17]

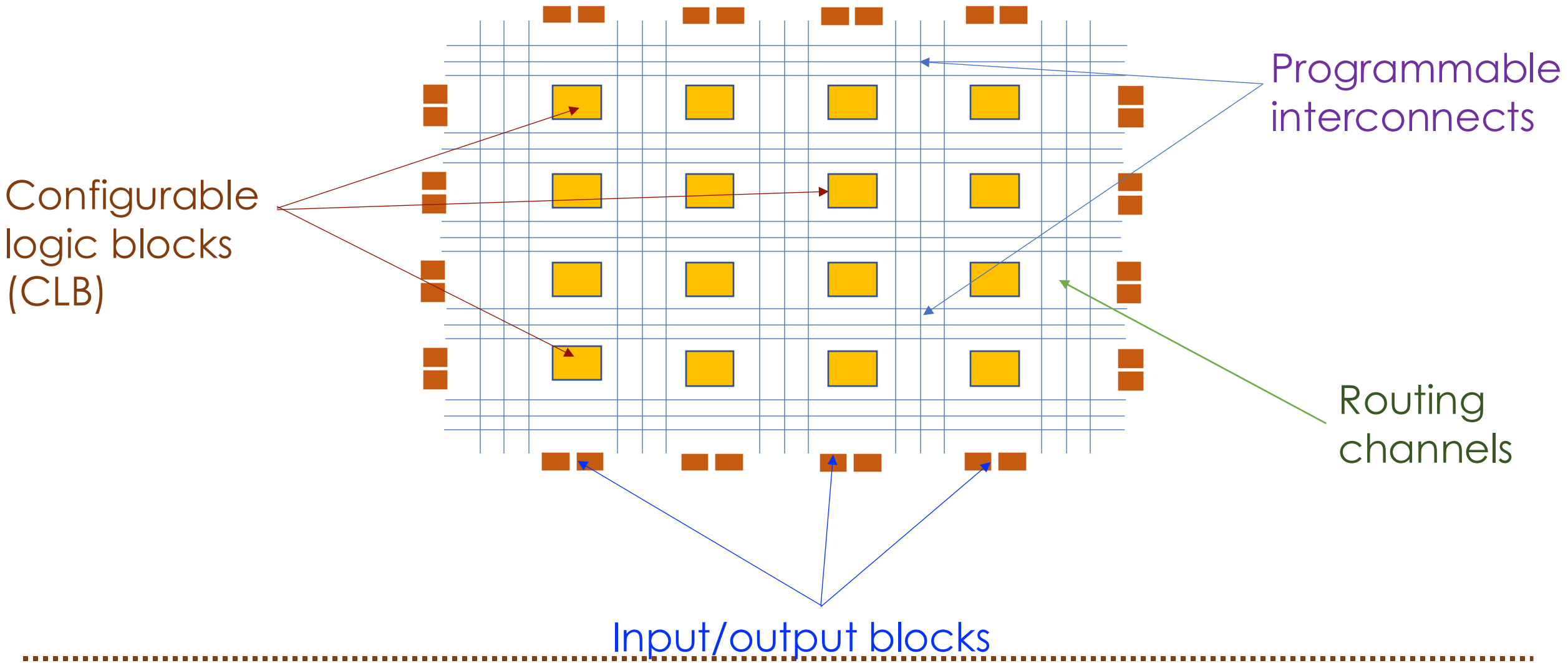
Source: *https://en.wikipedia.org/wiki/Field-programmable_gate_array*

FPGAs:

- Programmable hardware whose sub-component configuration can be changed even after fabrication: ***"field-programmable"***
- Has 2D array of logic gates in its architecture: ***"Gate Array"***
- A silicon **'breadboard'** of configurable logic gates, memories, transceivers, Digital Signal Processors (DSPs), registers (flip flops)



FPGA Architecture



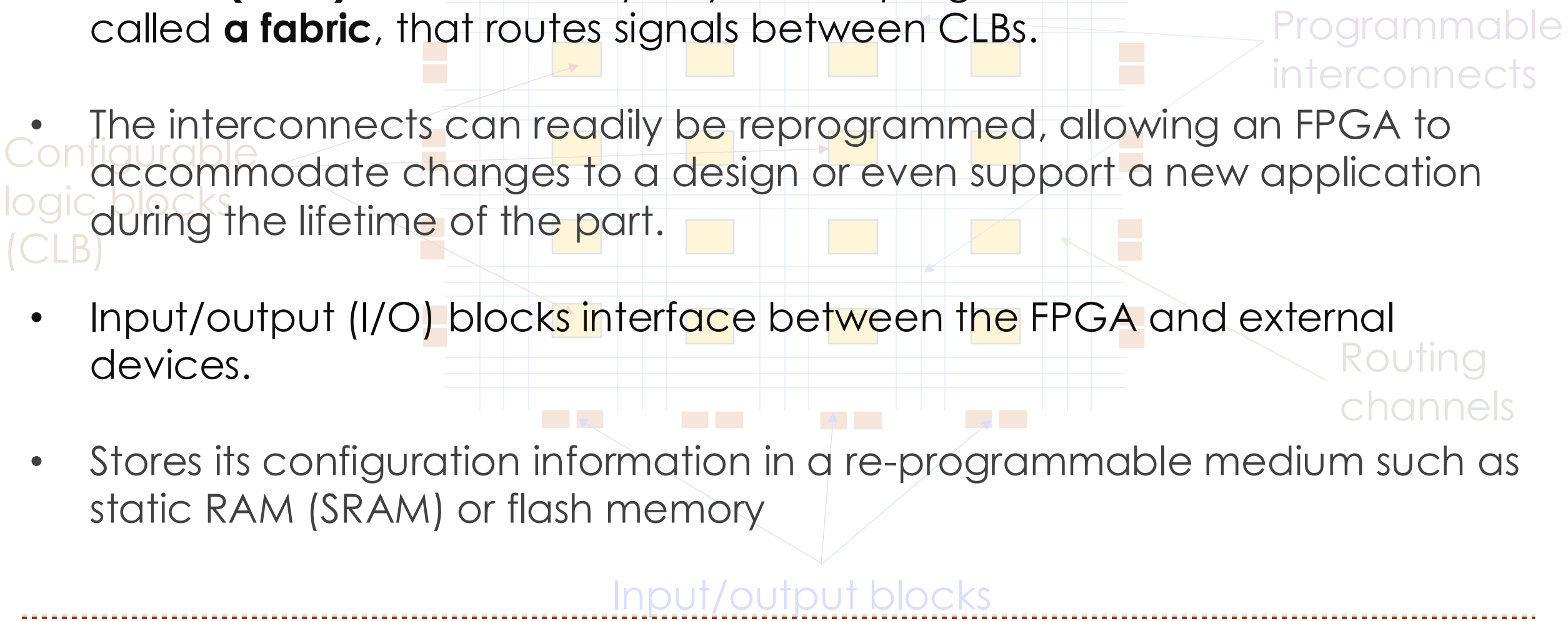
FPGA Architecture

- Contains thousands of fundamental elements called **configurable logic blocks (CLBs)** surrounded by a system of programmable interconnects, called **a fabric**, that routes signals between CLBs.

- The interconnects can readily be reprogrammed, allowing an FPGA to accommodate changes to a design or even support a new application during the lifetime of the part.

- Input/output (I/O) blocks interface between the FPGA and external devices.

- Stores its configuration information in a re-programmable medium such as static RAM (SRAM) or flash memory



FPGA Components

The basic structure of an FPGA is composed of:

- Look-up table (LUT)
- Flip-Flop (FF)
- Slices and CLBs
- Block Memory (BRAM)
- DSP Blocks
- Interconnect and routing resources: Wires & Input/Output (I/O) pads

Xilinx FPGAs – Phase-1 choice: V7 690T

Xilinx Multi-Node Product Portfolio Offering

45nm	28nm	20nm	16nm
SPARTAN-6	VIRTEX-7 KINTEX-7	VIRTEX UltraSCALE KINTEX UltraSCALE	VIRTEX UltraSCALE+ KINTEX UltraSCALE+

Currently Deployed

HL-LHC Prototypes

Product Tables and Product Selection Gu

Cost-Optimized Portfolio

Spartan-7	Spartan-6
Artix-7	Zynq-7000

7 Series

Spartan-7	Artix-7
Kintex-7	Virtex-7

UltraScale

Kintex UltraScale	Virtex UltraScale

UltraScale+

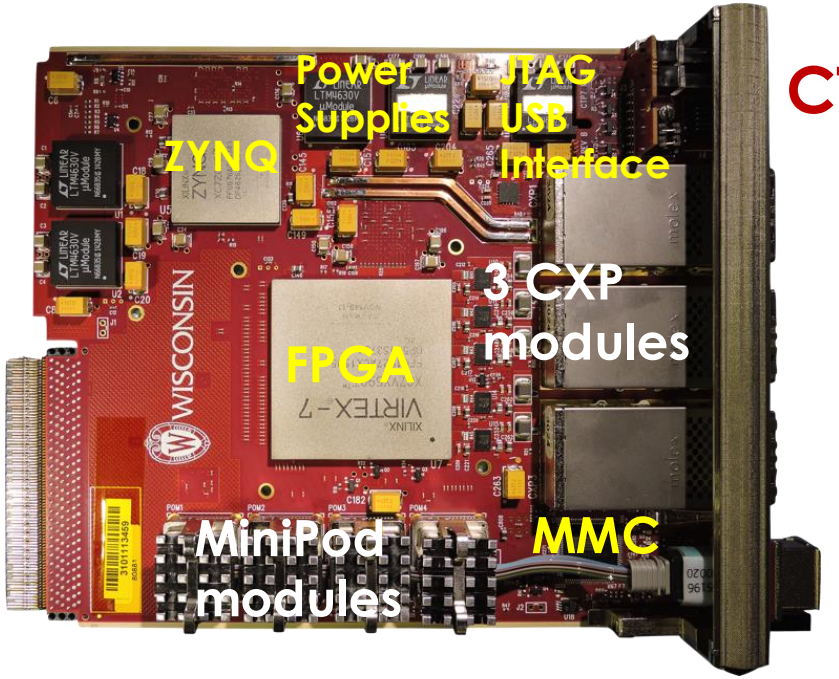
Kintex UltraScale+	Virtex UltraScale+

Decide wisely which FPGA to use as per your needs

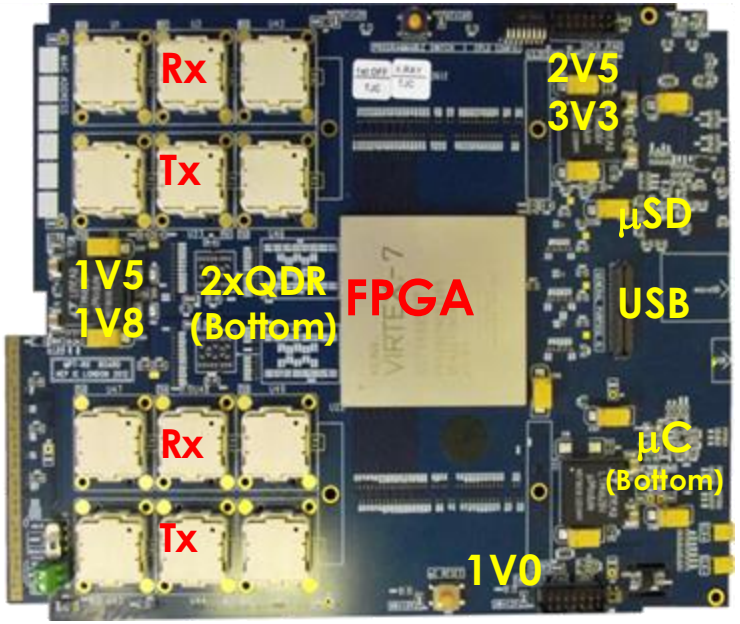
	Spartan-7	Artix-7	Kintex-7	Virtex-7
Max Logic Cells (K)	102	215	478	1,955
Max Memory (Mb)	4.2	13	34	68
Max DSP Slices	160	740	1,920	3,600
Max Transceiver Speed (Gb/s)	--	6.6	12.5	28.05
Max I/O Pins	400	500	500	1,200

Speed grade: maximum propagation delay for critical paths in the FPGA fabric or I/O operations

Trigger Processor Boards



CTP7

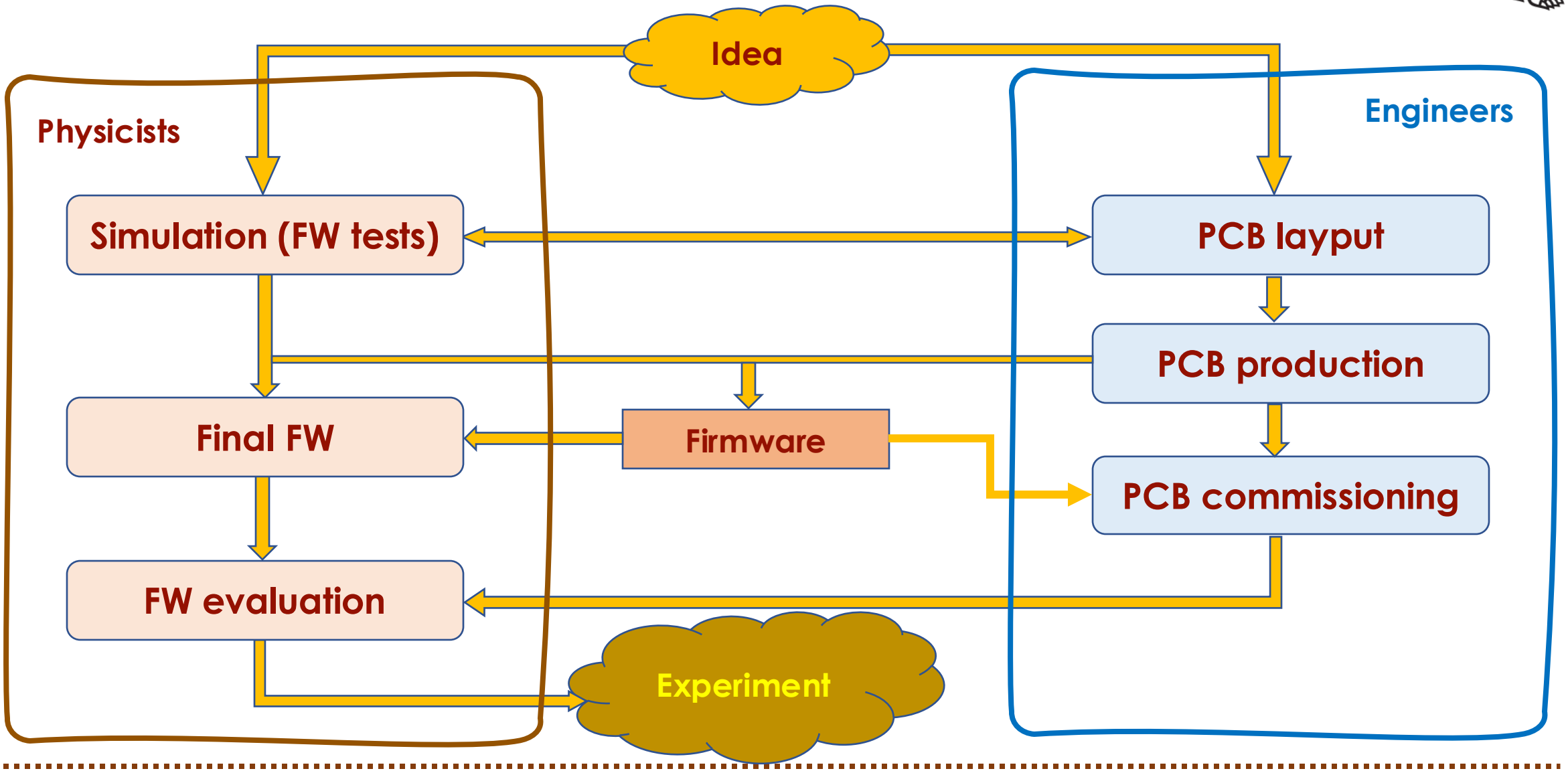


MP7

Calorimeter Trigger Processor(CTP7 – left), and Master Processor (MP7 - right)

- **CTP7 (Layer-1) – mTCA Single Virtex 7 FPGA, 67 optical inputs, 48 outputs, 12 RX/TX backplane**
  - Virtex 7 allows 10 Gb/s link speed on 3 CXP(36 TX & 36 RX) and 4 MiniPODs (31 RX & 12 TX)
  - ZYNQ processor running Xilinx PetaLinux for service tasks, including virtual JTAG cable
- **MP7 (Layer-2) – mTCA Single Virtex 7 FPGA, up to 72 input & output links**
  - Virtex 7 has 72 input and output links at 10 Gb/s
  - Dual 72 or 144MB QDR RAM clocked at 500 MHz

Workflow during FPGA development



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Questions?